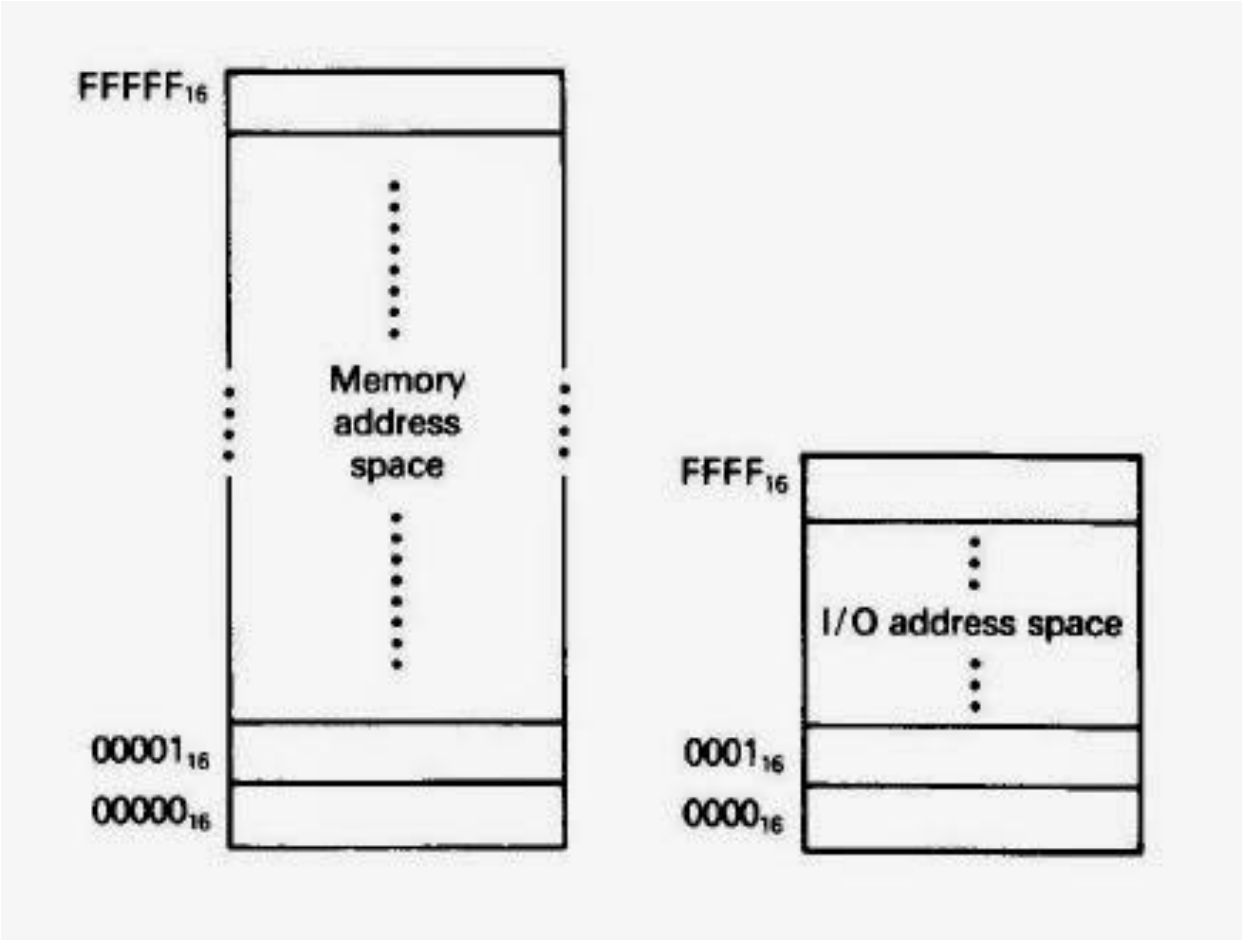
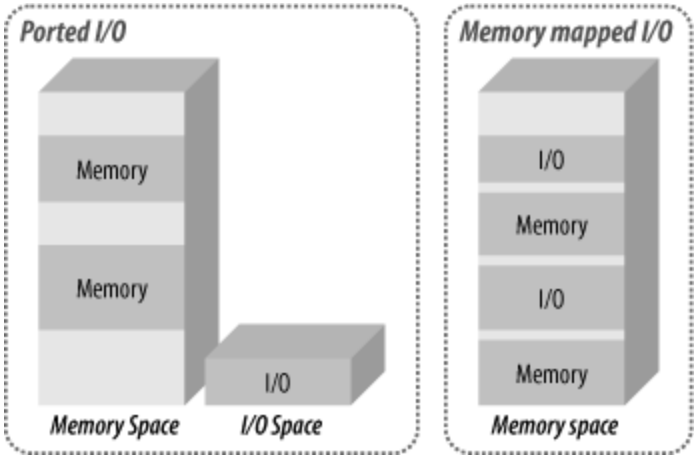
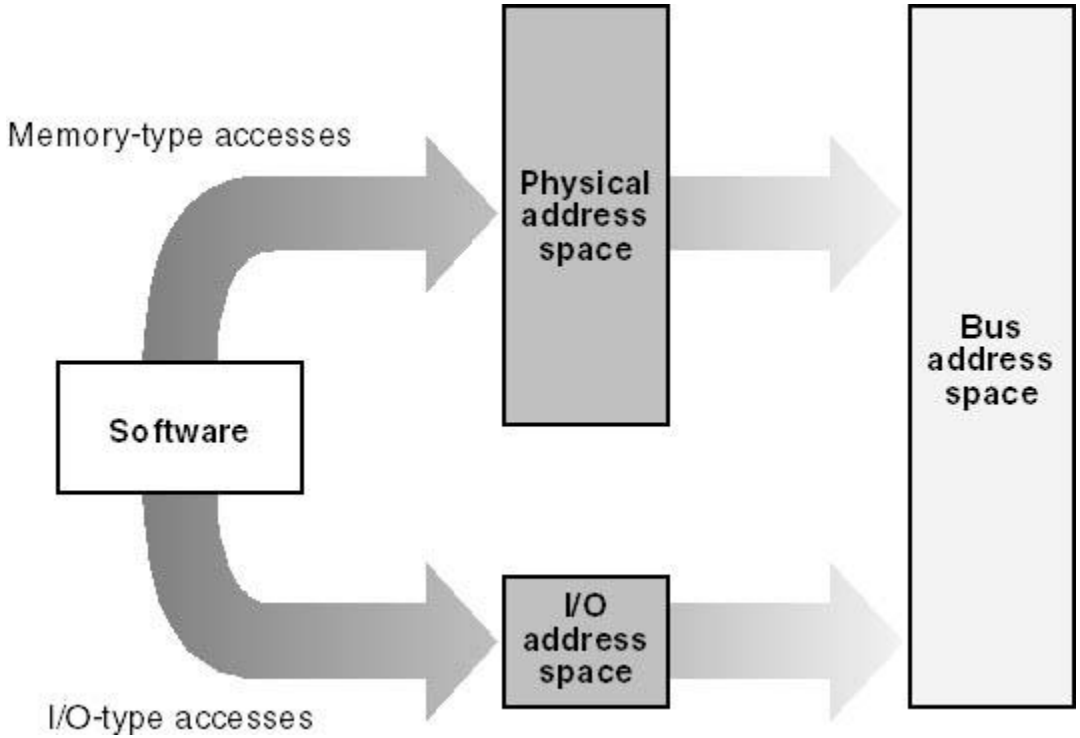
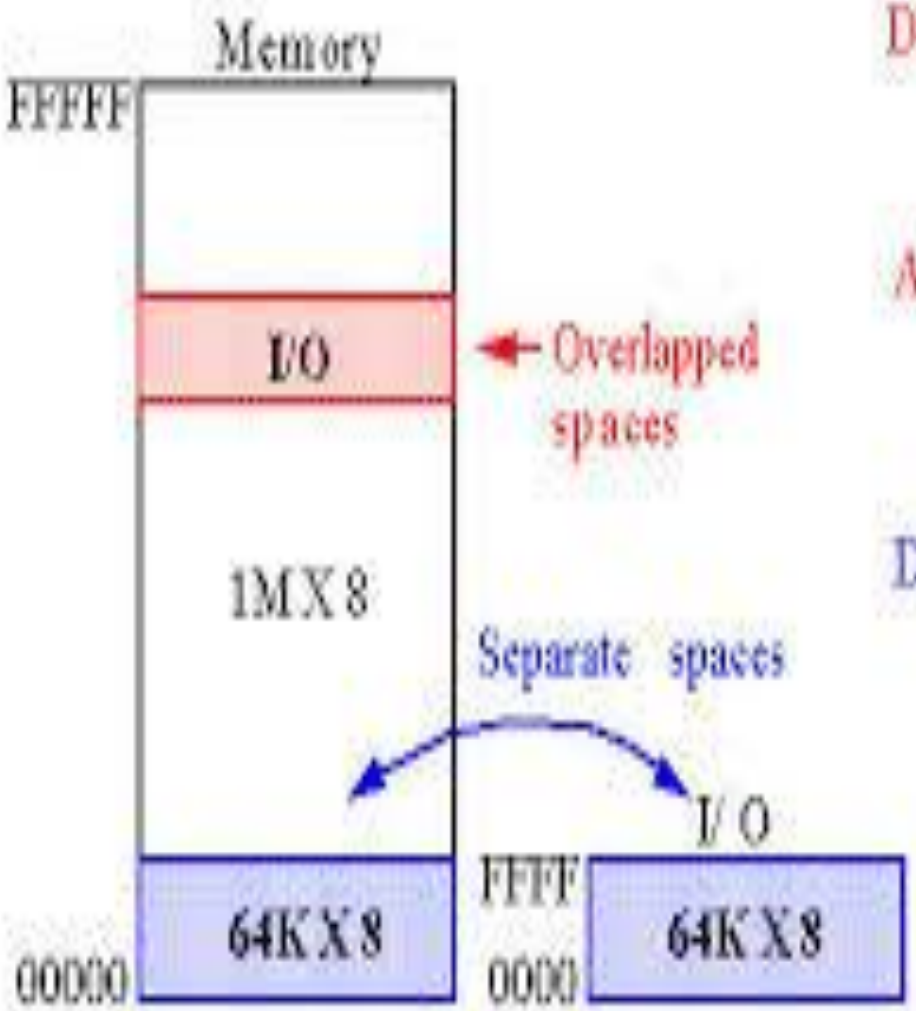
Topic 5. Allocation of program's segments inside the memory. Linking of a program. The main methods of work with the "turbo-debugger".

1. Why is it necessary to use a stack in a program?
2. Describe the stack organization.
3. What size should have a stack?
4. Describe the apparatus organization of interrupts.
5. Describe the service of interrupt procedure.
6. I/O system.


FFFFF16
Memory address space
00001₁₆
00000₁₆
FFFF16
I/O address space
0001₁₆
0000₁₆


Ported I/O
Memory
Memory
I/O
Memory Space
I/O Space
Memory mapped I/O
I/O
Memory
I/O
Memory
Memory space


Memory-type accesses
Physical address space
Bus address space
Software
I/O address space
I/O-type accesses



Disadvantage:

A portion of the memory space is used for I/O devices.

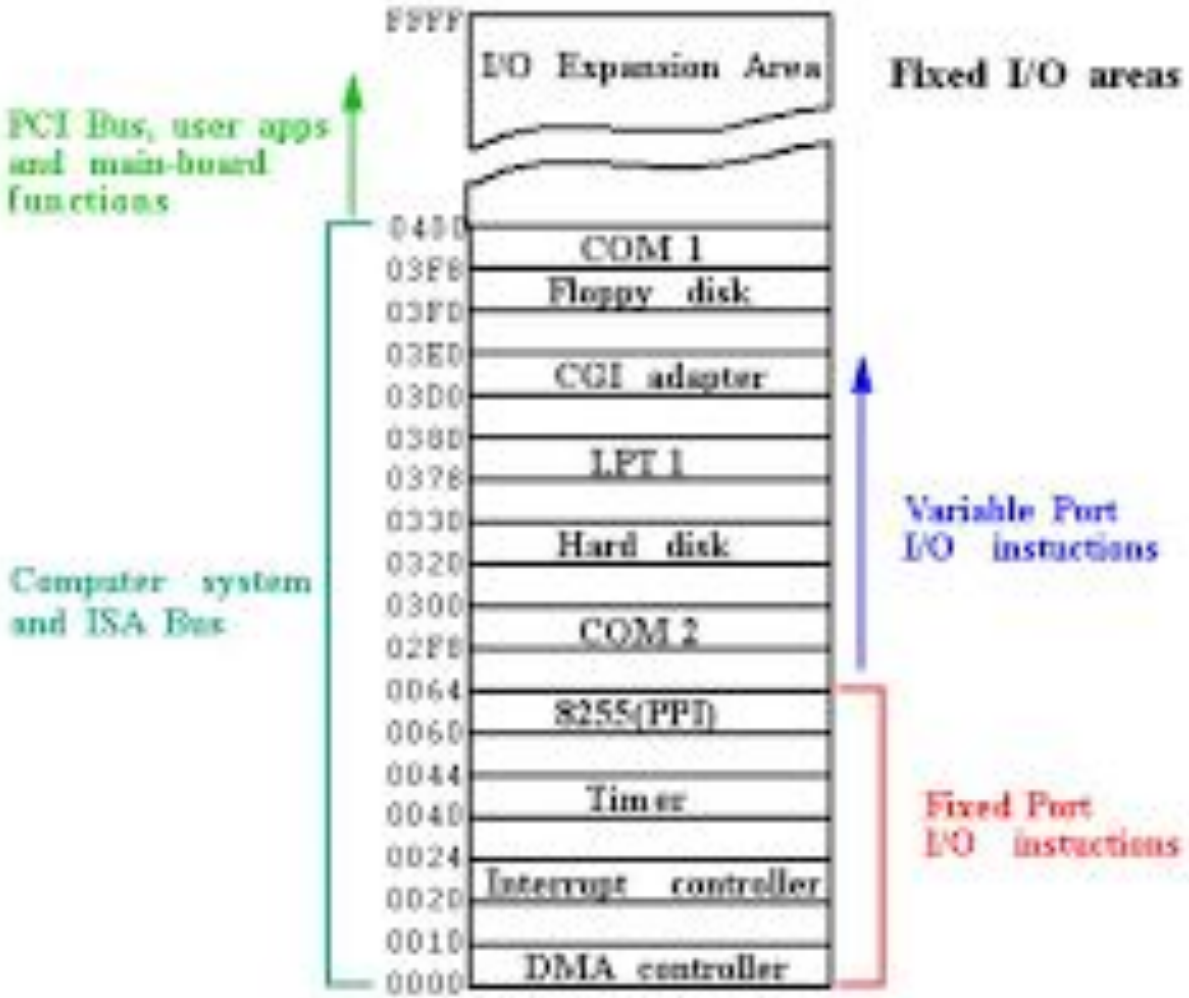
Advantage:

$\overline{IORC}$ and $\overline{IOWC}$ not required. Any data transfer instruction.

Disadvantage:

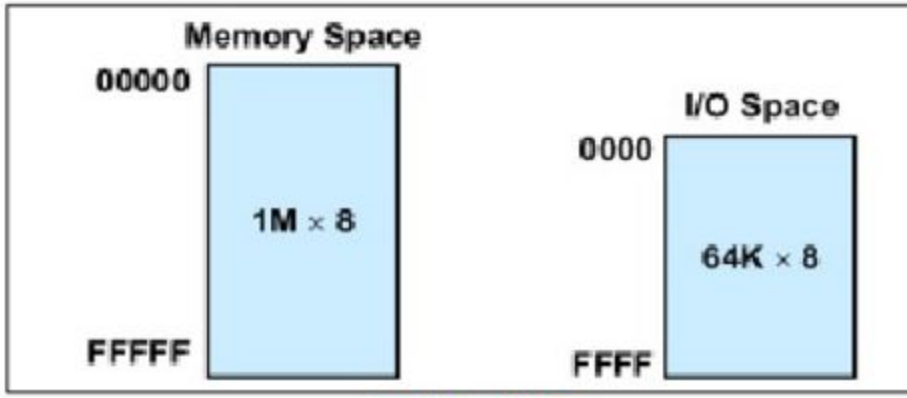
Hardware using M/$\overline{IO}$ and W/$\overline{R}$ needed to develop signals $\overline{IORC}$ and $\overline{IOWC}$.

Requires IN, OUT, INS and OUTS

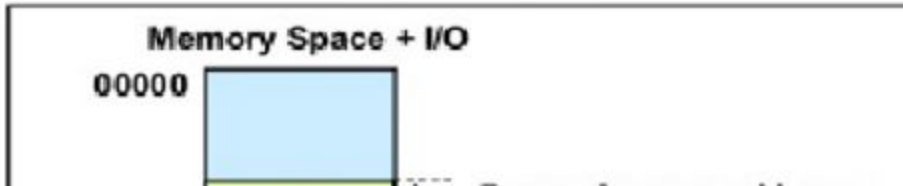

FFFF
I/O Expansion Area
Fixed I/O areas
PCI Bus, user apps and main-board functions
0400
COM 1
03F8
Floppy disk
03F0
03E0
CGI adapter
03D0
0380
LPT 1
0378
0330
Hard disk
0320
0300
COM 2
02F8
0064
8255(PPI)
0060
0044
Timer
0040
0024
Interrupt controller
0020
0010
DMA controller
0000
Computer system and ISA Bus
Variable Port I/O instuctions
Fixed Port I/O instuctions

[redacted]

Isolated vs. Memory Mapp

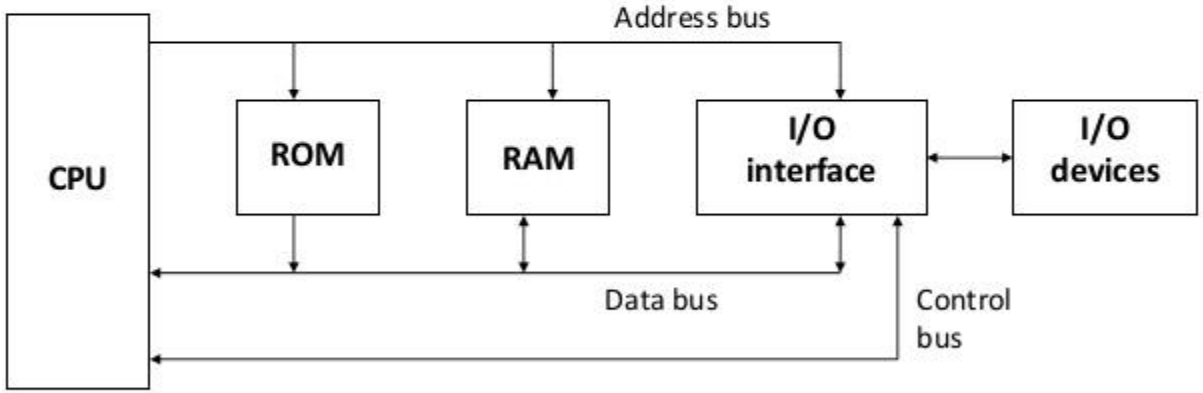


Isolated I/O



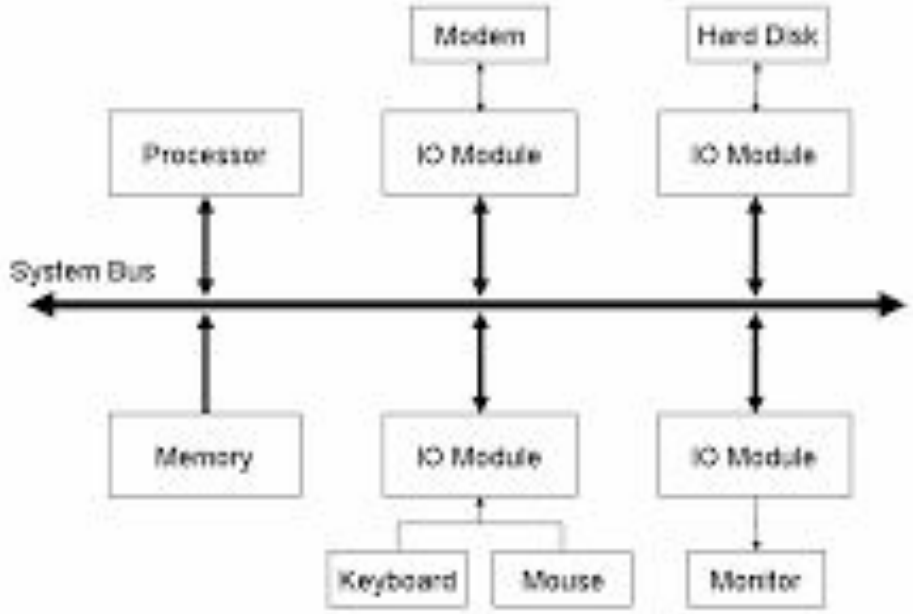
BLOCK DIAGRAM OF A BASIC COMPUTER SYSTEM

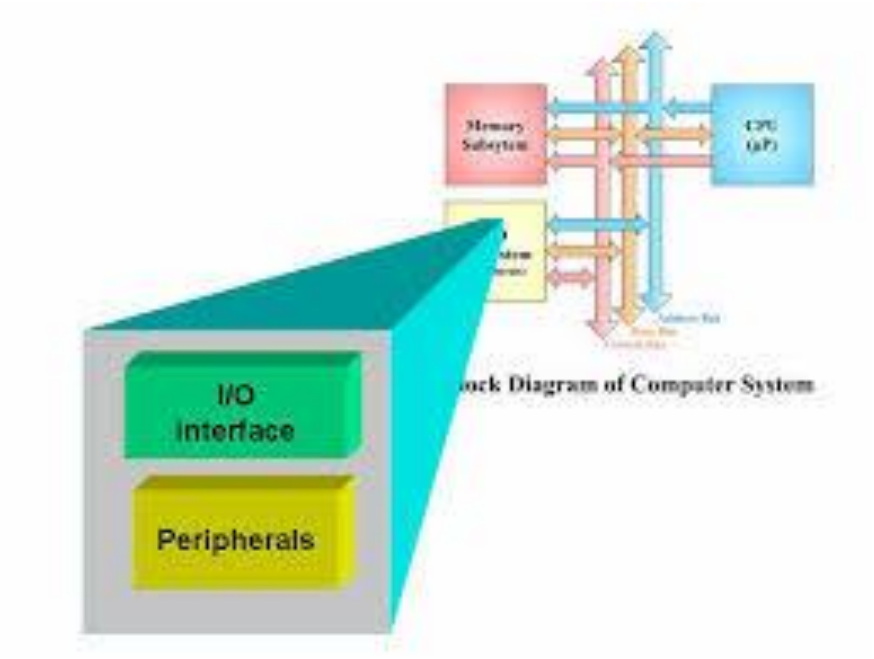
Basic computer system consist of a Central processing unit (CPU), memory (RAM and ROM), input/output (I/O) unit.

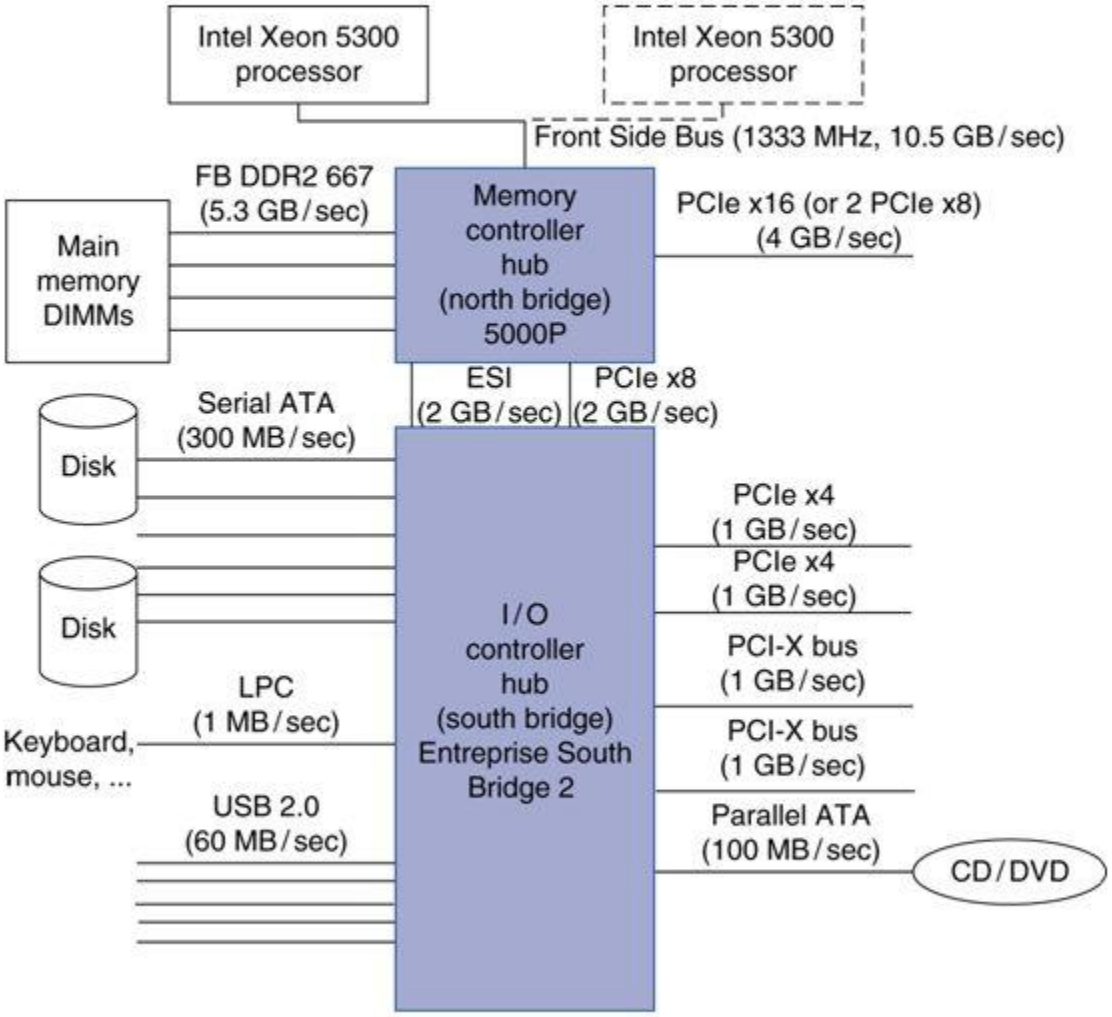


Block diagram of a basic computer system

I/O Subsystem Block Diagram

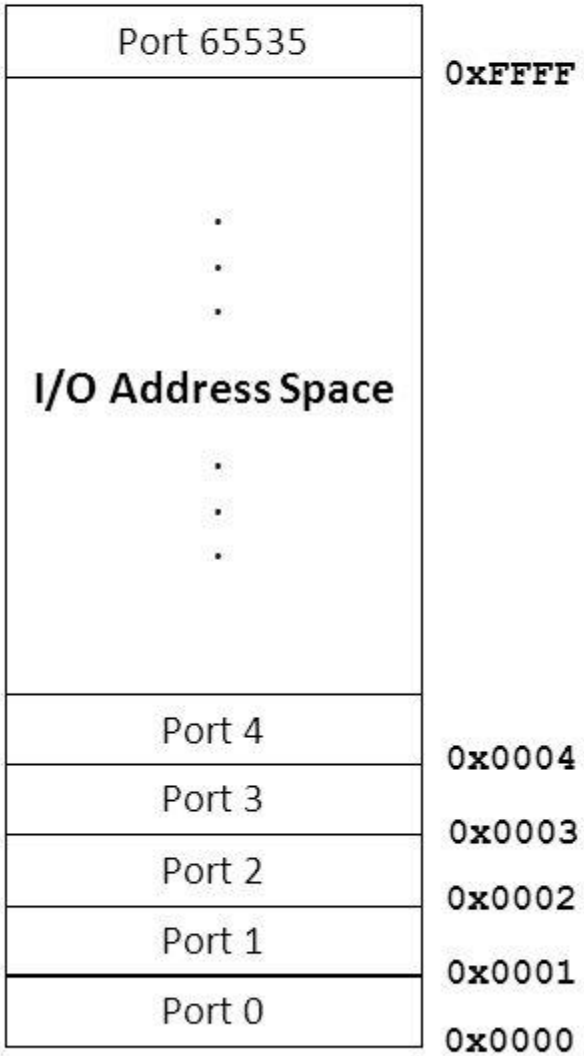



I/O
Interface
Peripherals


Intel Xeon 5300 processor
Intel Xeon 5300 processor
Front Side Bus (1333 MHz, 10.5 GB/sec)
FB DDR2 667 (5.3 GB/sec)
Main memory DIMMs
Memory controller hub (north bridge) 5000P
PCIe x16 (or 2 PCIe x8) (4 GB/sec)
ESI (2 GB/sec)
PCIe x8 (2 GB/sec)
Serial ATA (300 MB/sec)
Disk
Disk
I/O controller hub (south bridge) Entreprise South Bridge 2
PCIe x4 (1 GB/sec)
PCIe x4 (1 GB/sec)
PCI-X bus (1 GB/sec)
PCI-X bus (1 GB/sec)
Parallel ATA (100 MB/sec)
CD/DVD
LPC (1 MB/sec)
Keyboard, mouse, ...
USB 2.0 (60 MB/sec)

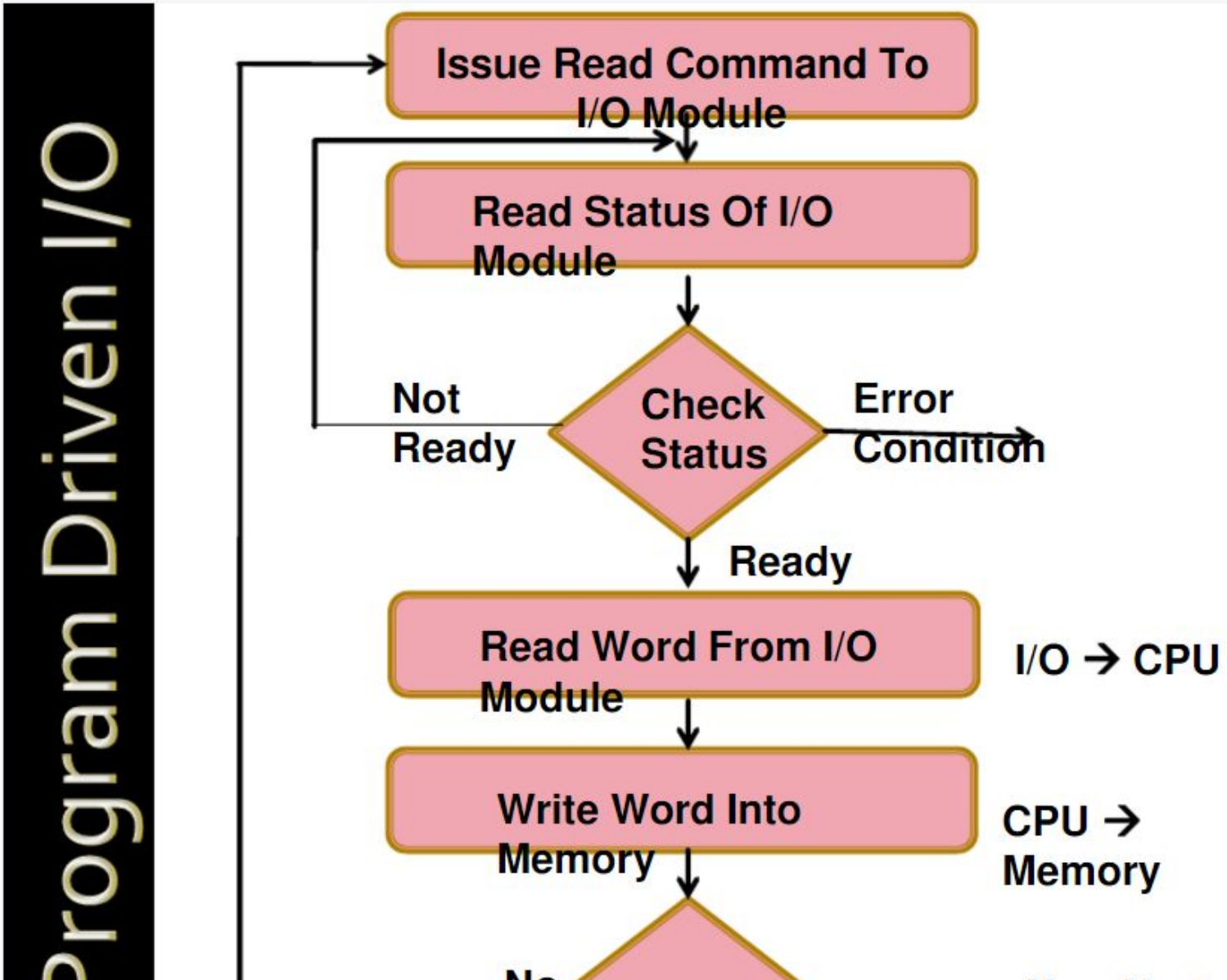
Port I/O Address Space

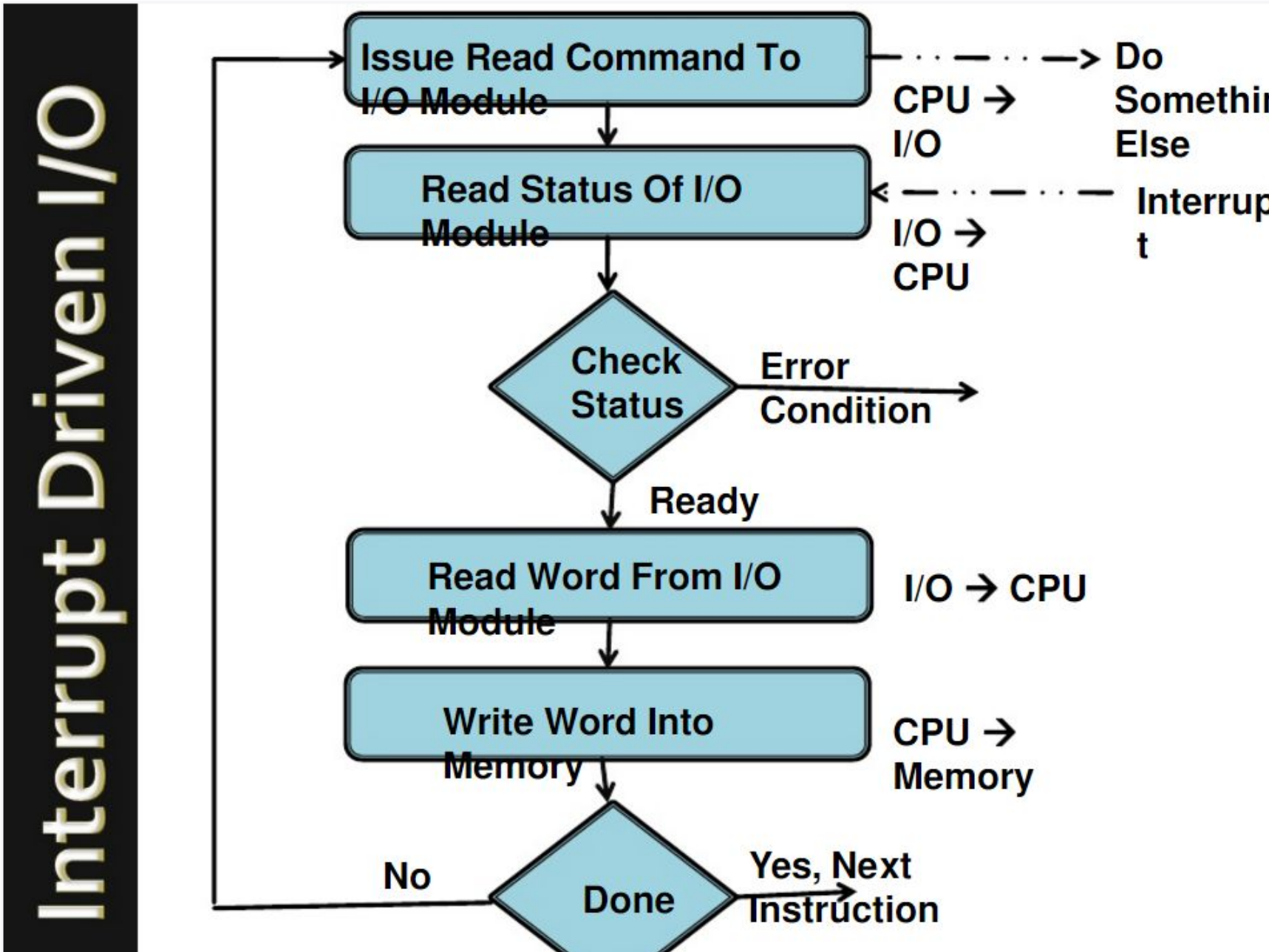
- Software and hardware architectures of x86 architecture support a separate address space called “I/O Address Space”
  - Separate from memory space
- Access to this separate I/O space is handled through a set of I/O instructions
  - IN,OUT, INS, OUTS
- Access requires Ring0 privileges
  - Access requirement does not apply to all operating modes (like Real-Mode)
- The processor allows 64 KB+3 bytes to be addressed within the I/O space
- Harkens back to a time when memory was not so plentiful
- You may never see port I/O when analyzing high-level applications, but in systems programming (and especially BIOS) you will see lots of port I/O
- One of the biggest impediments to understanding what's going on in a BIOS

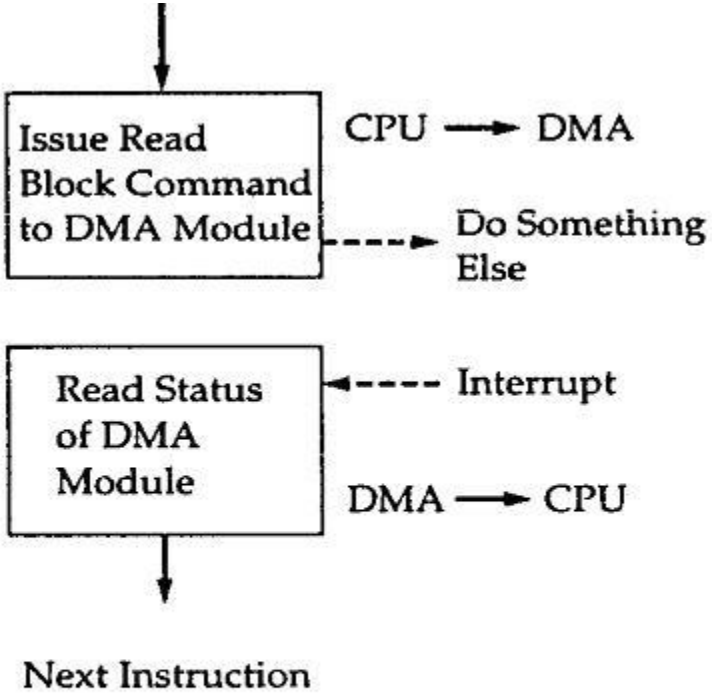


ntel Programmer’s guide, Vol 1, 16.1

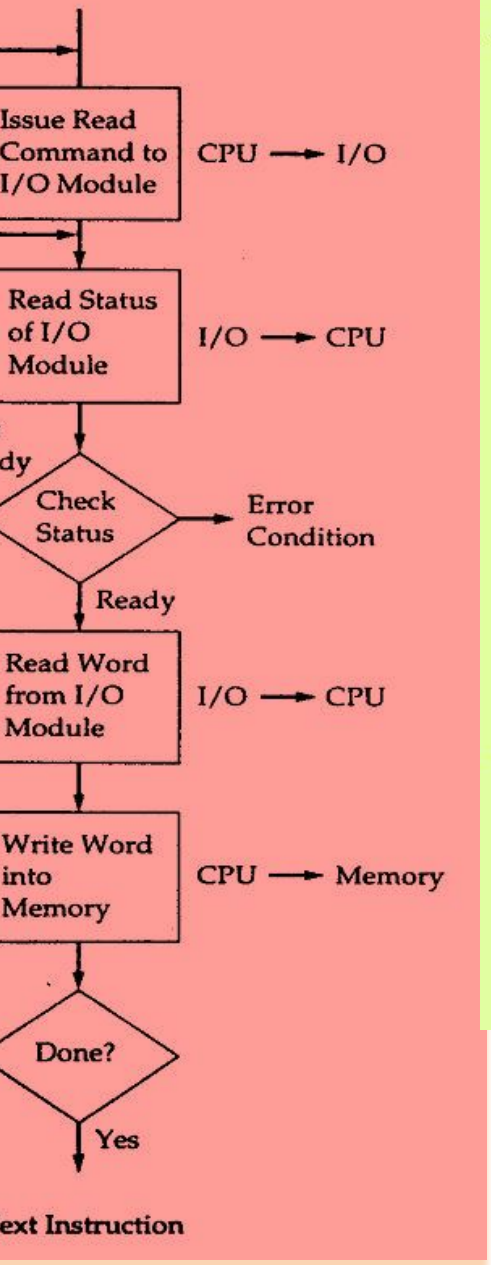
- Hence the processor is kept busy needlessly.

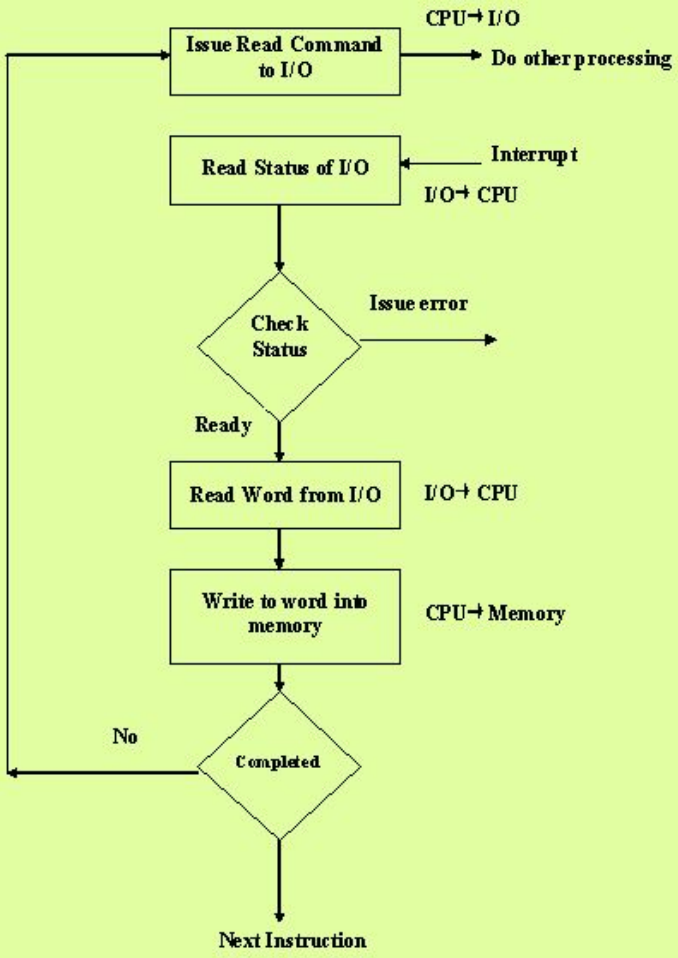


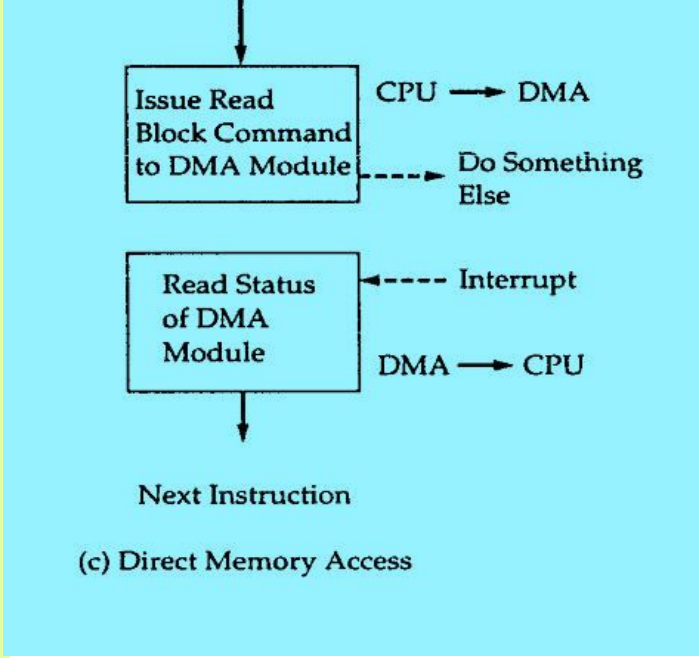

Interrupt Driven I/O
Issue Read Command To I/O Module
CPU → I/O
Do Somethin Else
Read Status Of I/O Module
I/O → CPU
Interrup t
Check Status
Error Condition
Ready
Read Word From I/O Module
I/O → CPU
Write Word Into Memory
CPU → Memory
Done
No
Yes, Next Instruction



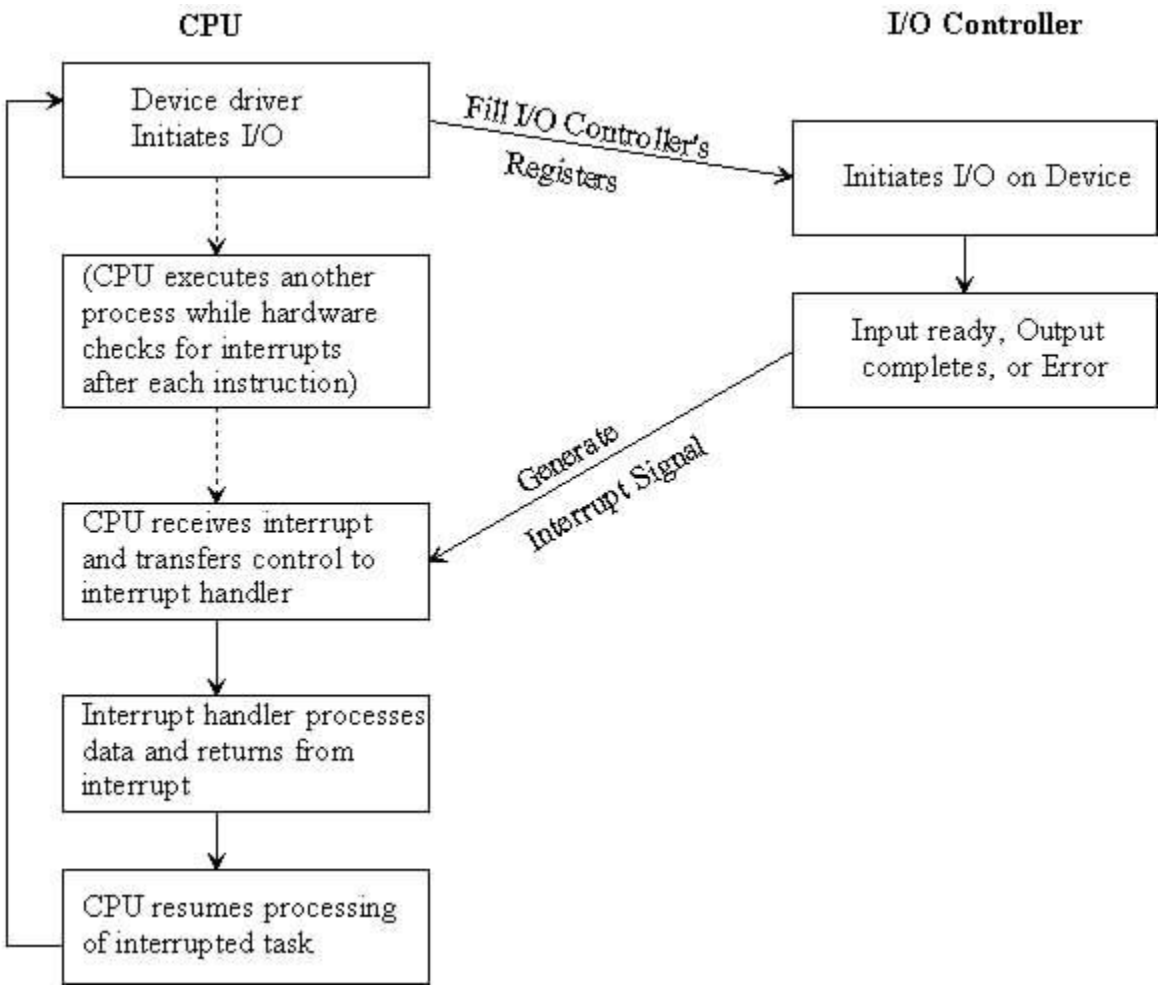
(c) Direct Memory Access





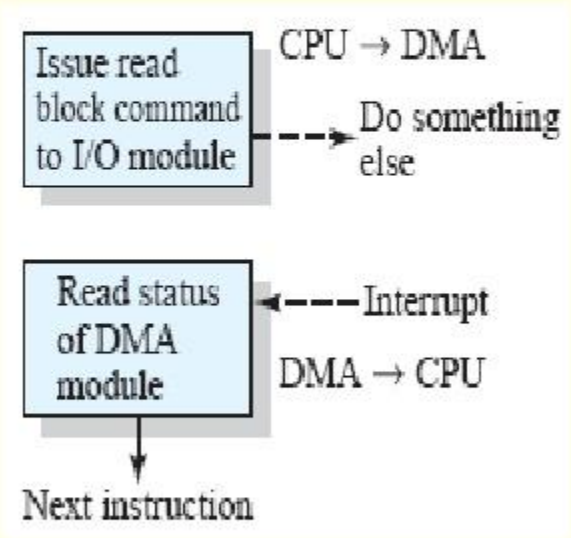


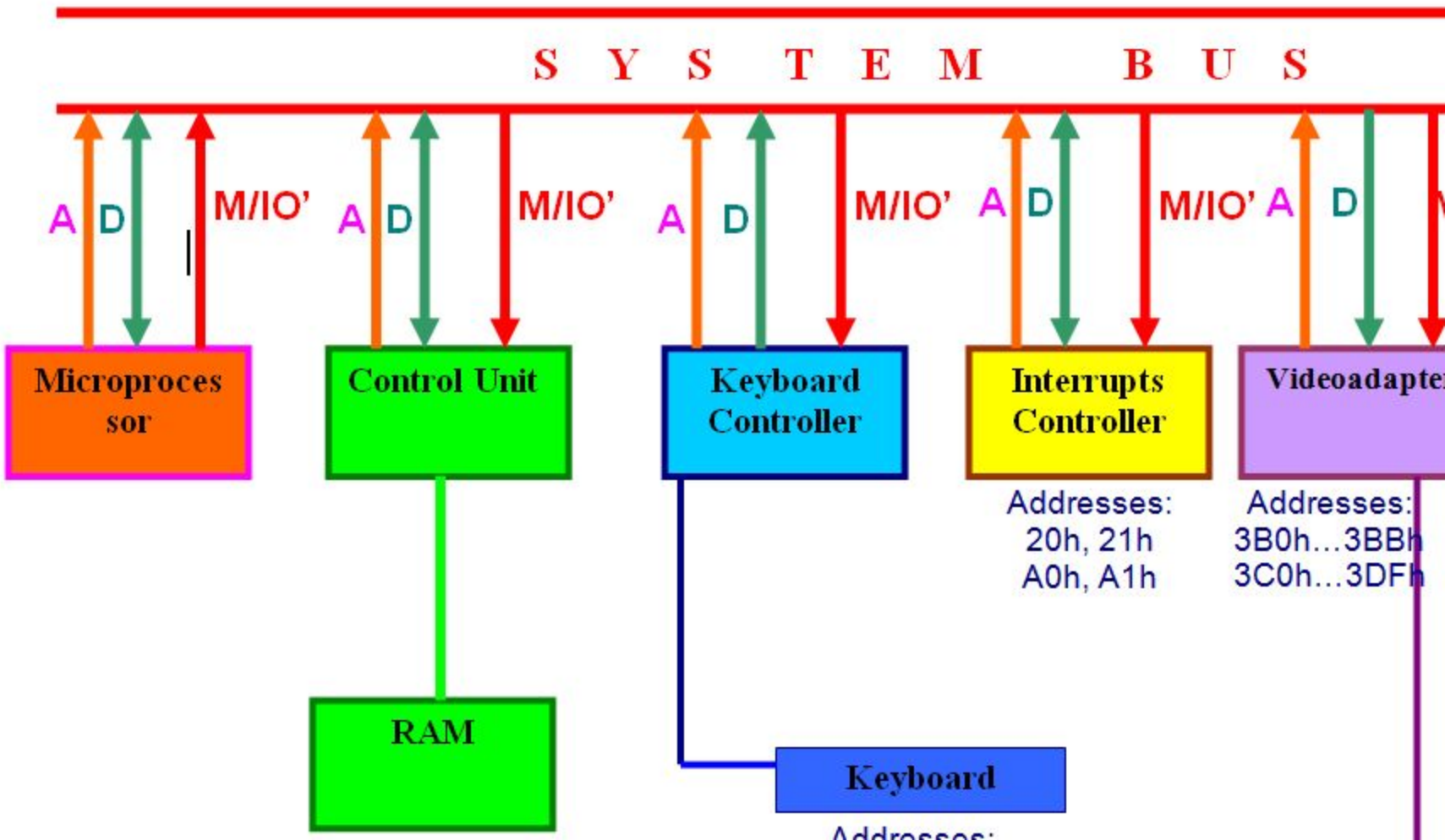
(c) Direct Memory Access


CPU
I/O Controller
Device driver Initiates I/O
Fill I/O Controller's Registers
Initiates I/O on Device
(CPU executes another process while hardware checks for interrupts after each instruction)
Input ready, Output completes, or Error
Generate Interrupt Signal
CPU receives interrupt and transfers control to interrupt handler
Interrupt handler processes data and returns from interrupt
CPU resumes processing of interrupted task

Direct Memory Access (DMA)

- I/O exchanges occur directly with memory
  - Requires DMA module on system bus
  - Capable of mimicking CPU and taking over control of system from CPU
  - DMA will use bus when
    - Processor does not require it OR
    - Must force processor to suspend operation temporarily– called cycle stealing
- An interrupt is sent when the task is complete
- The processor is only involved at the beginning and end of the transfer




S Y S T E M B U S
A D M/IO'
A D M/IO'
A D M/IO'
A D M/IO'
A D M/IO'
Microprocessor
Control Unit
Keyboard Controller
Interrupts Controller
Videoadapte
Addresses:
20h, 21h
A0h, A1h
Addresses:
3B0h…3BBh
3C0h…3DFh
RAM
Keyboard
Addresses:

The 8086 can generate 16-bit of I/O address. Thus it can address up to 64 Kbyte I/O locations or 32 K word I/O locations.
The 16-bit I/O address appears on A_0 to A_15 address lines; A_16 to A_19 lines are at logic 0 during the I/O operations.
The 16-bit DX register is used as 16-bit I/O address pointer to address up to 64 IC devices in in-direct addressing mode.
The 1/0 instructions with direct addressing mode can directly address one or two of the 256 I/O byte locations in page 0 of the 1/0 address space.