Modulul de comunicare USART

I. Structura modulului USART încorporat
II. Modurile de funcționare
III. Regiștrii de control

Modulul USART (Universal Synchronous and Asynchronous Receiver Transmitter) se utililizează pentru comunicarea între două sau mai multe dispozitive (PC, sisteme de control cu microcontroler etc).

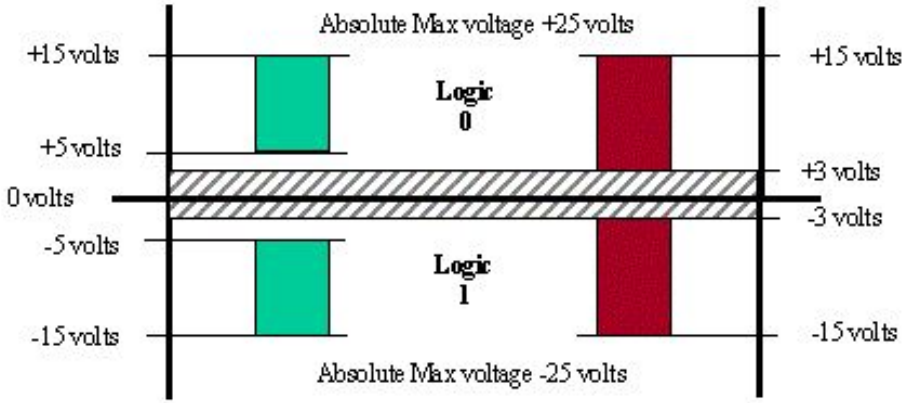
Dacă în calitate de mediu se utilizează RS-485 distanța între noduri poate fi de pînă la 100m

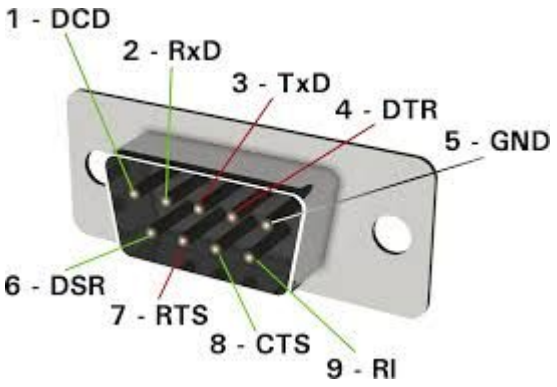
În calitate de mediu de transmitere pot fi utilizate transmițătoare:

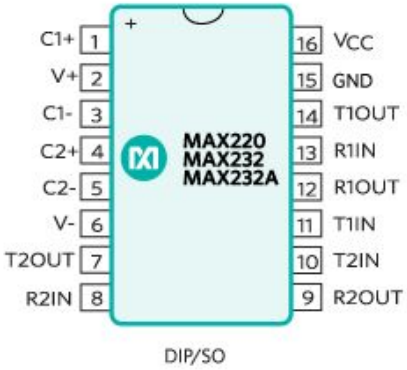
- RS-232
- RS-422
- RS-485

Standarde TIA/EIA (*Telecommunications Industry Association and Electronic Industries Alliance*)

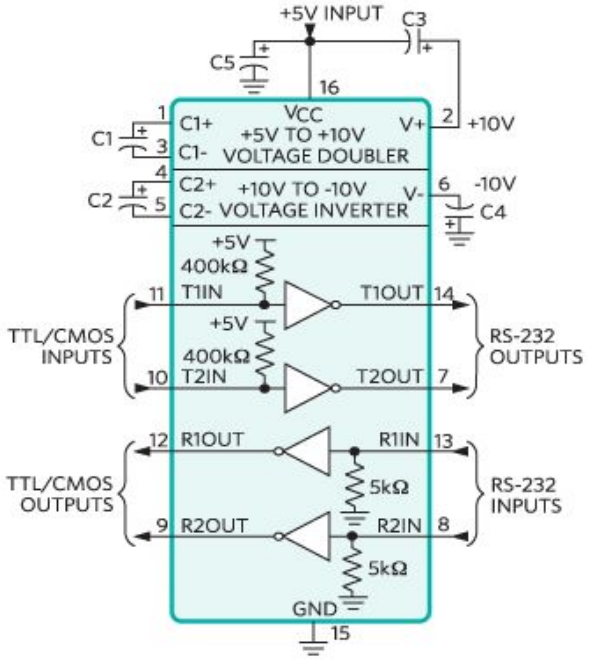
RS - 232



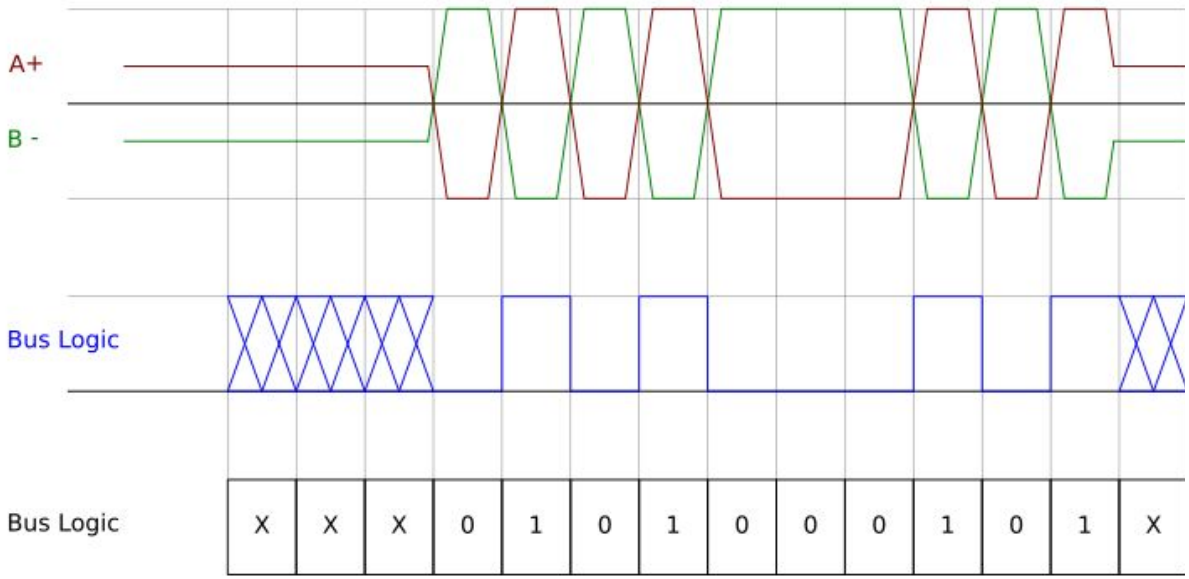


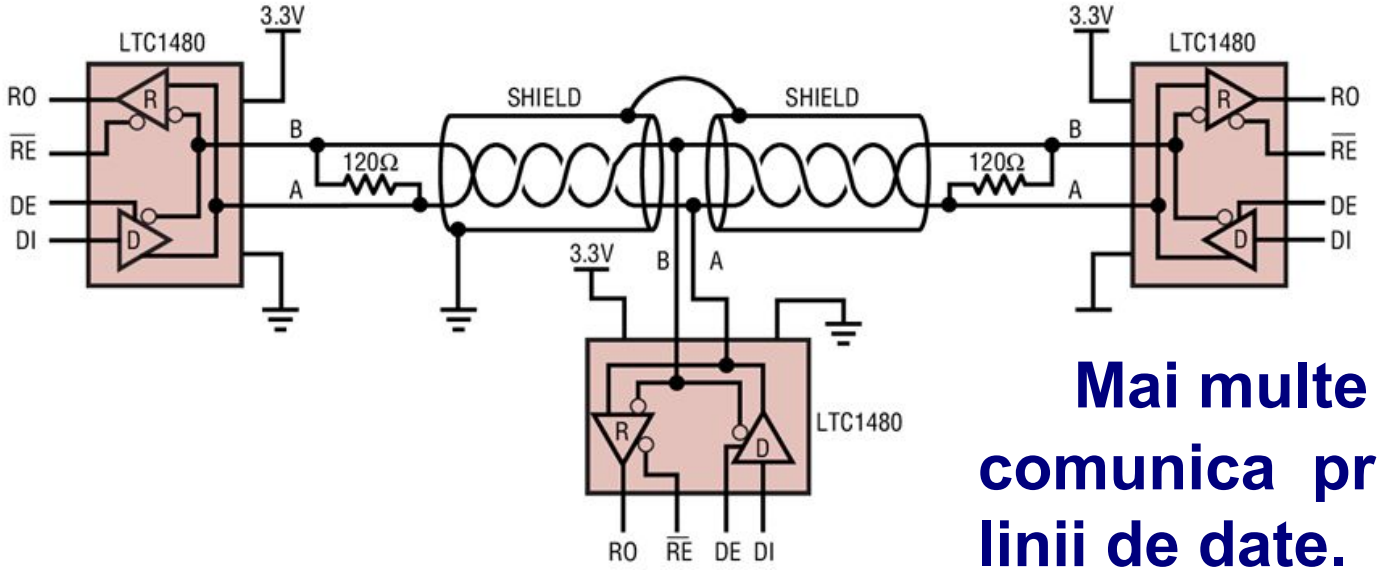


CAPACITANCE (µF)					
DEVICE	C1	C2	C3	C4	C5
MAX220	0.047	0.33	0.33	0.33	0.33
MAX232	1.0	1.0	1.0	1.0	1.0
MAX232A	0.1	0.1	0.1	0.1	0.1



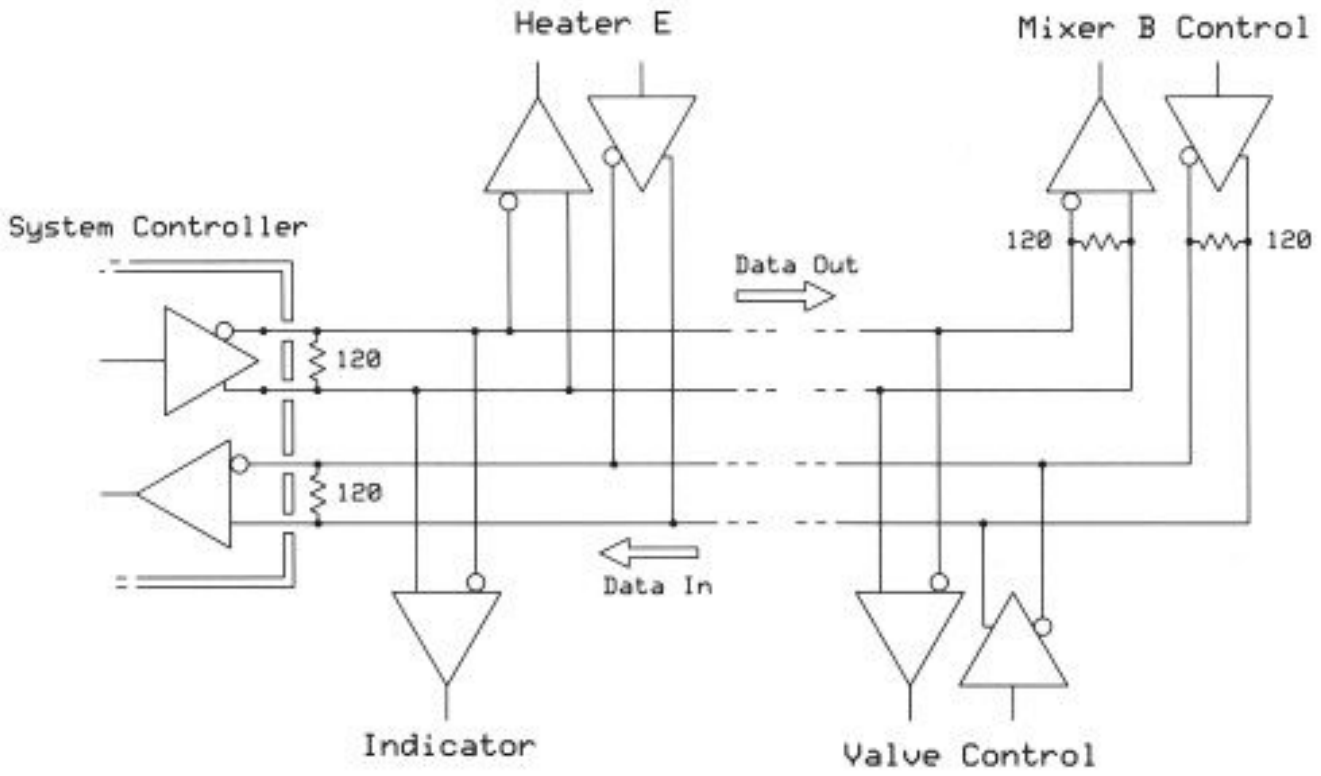
Standardul RS485 utilizează transmițătoare diferențiale





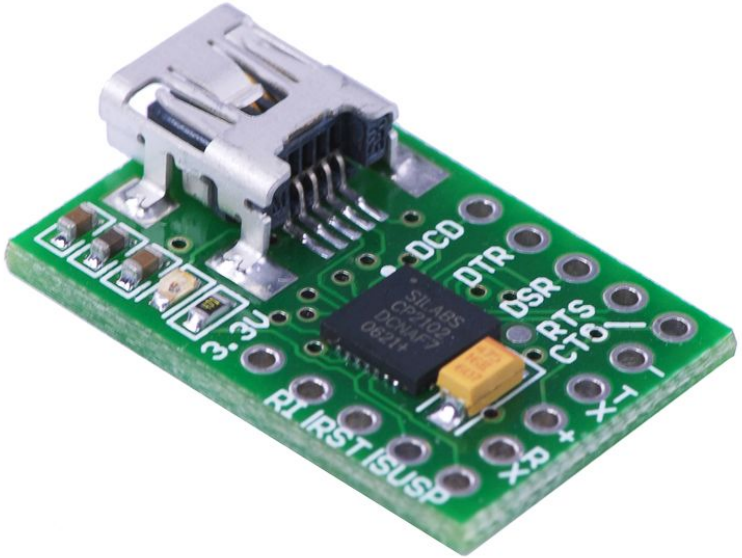
Mai multe noduri pot comunica prin aceleași linii de date.

Interfața RS-422 utilizează 2 perechi de linii diferențiale

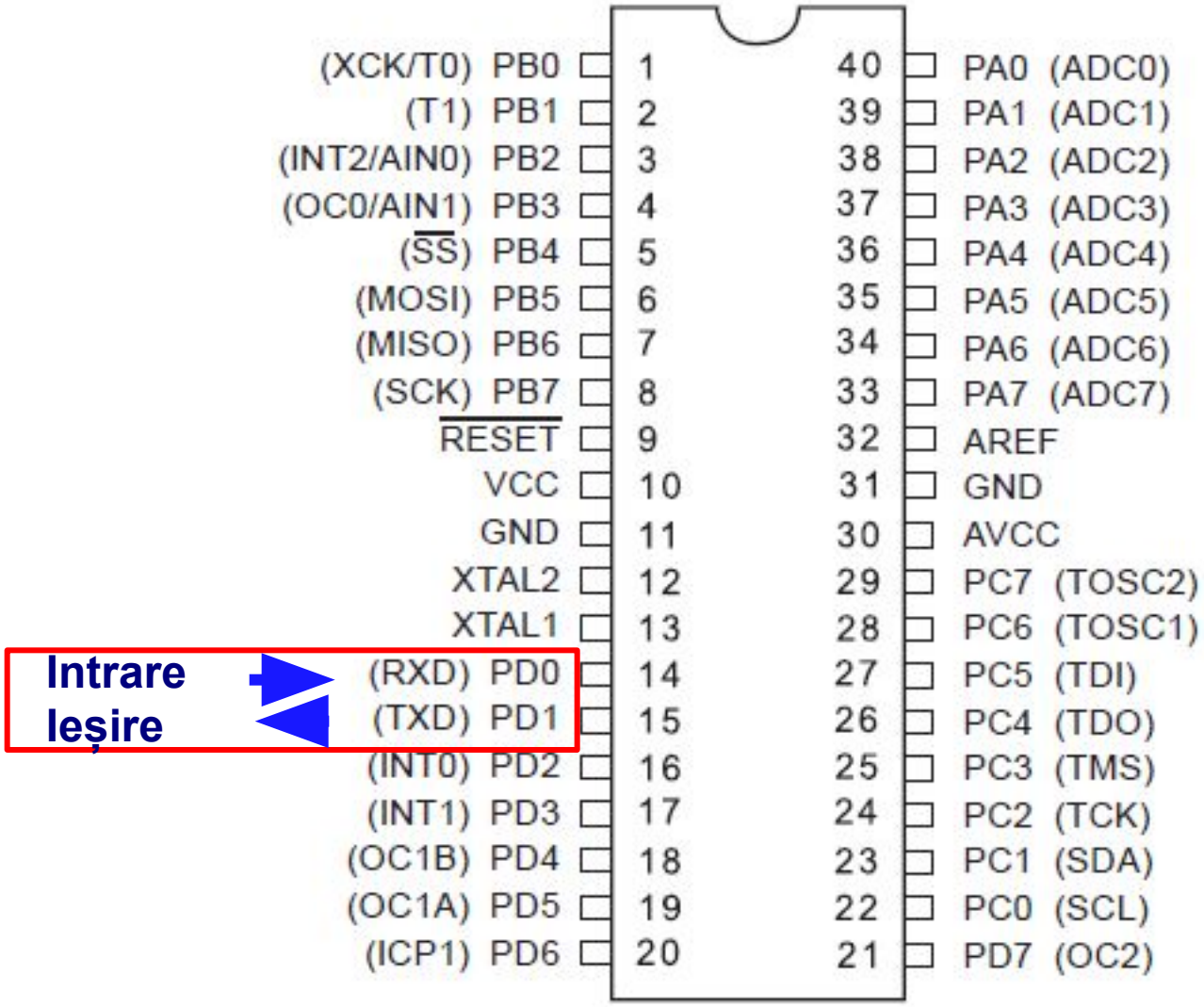


pentru conectarea MCU la Host (PC/Tab., etc) pot fi utilizate convertoare UART to USB:

- FTDI (FT232xx…)
- SILABS (CP2102)
- WCH (CH341…)



I. Structura Modulului USART încorporat



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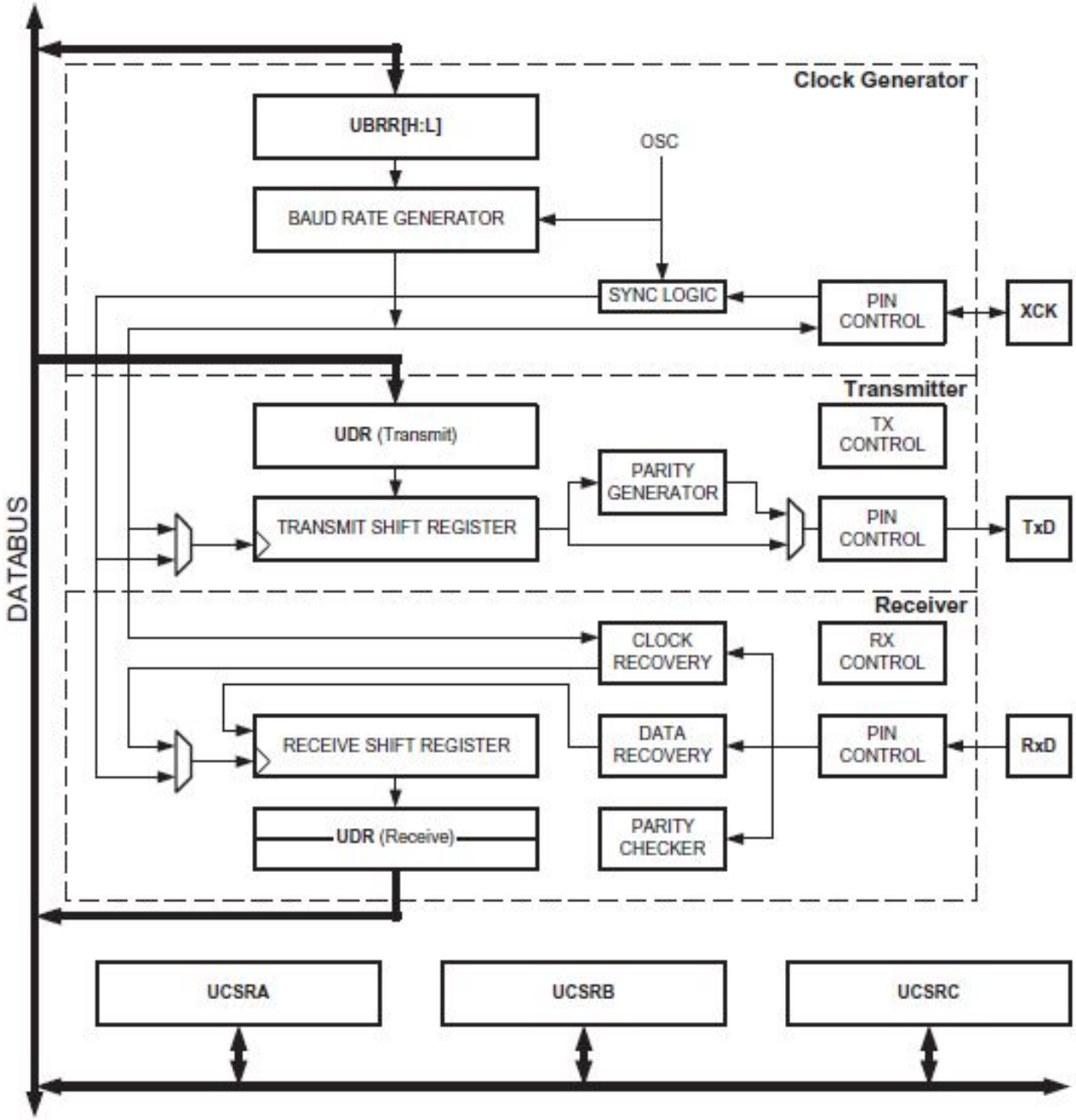
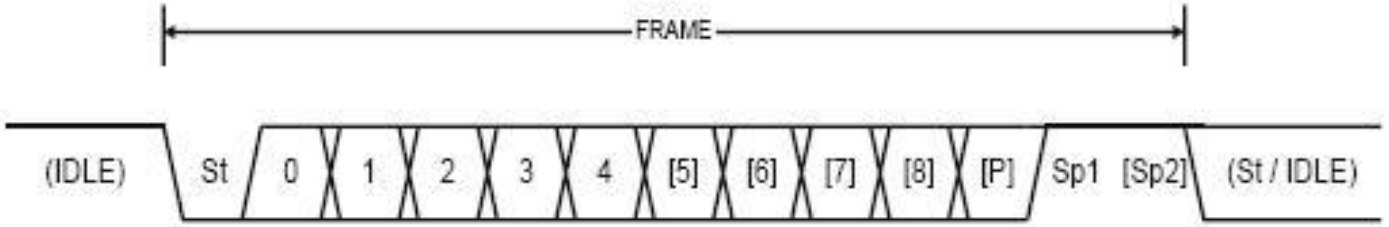


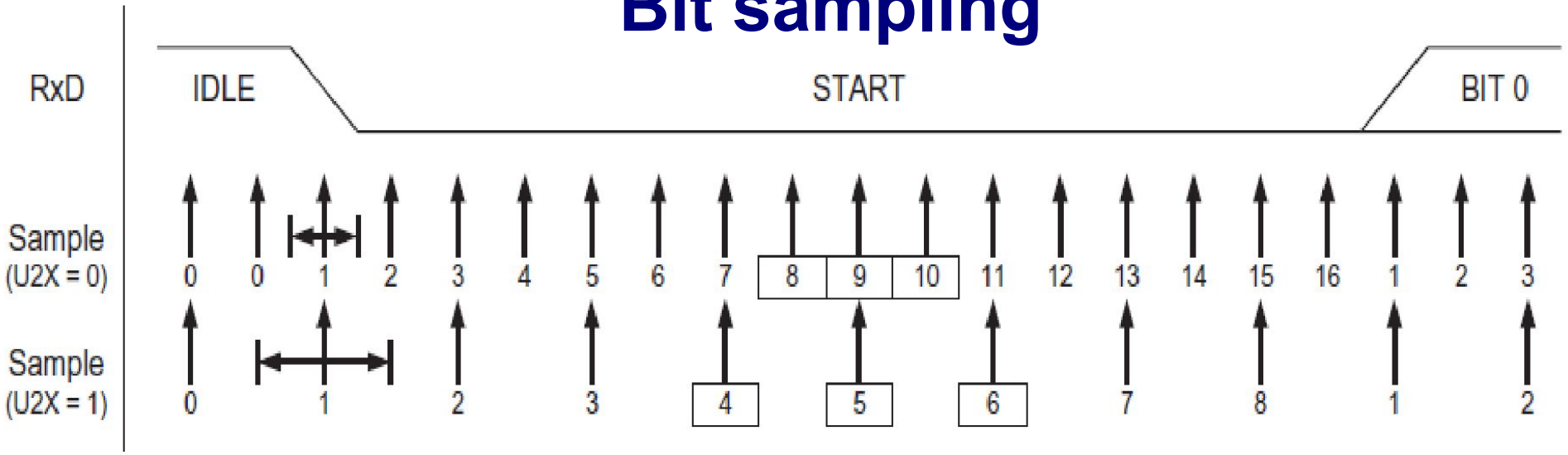
FIgure 22-4. Frame Formats



St	Start bit, always low.
(n)	Data bits (0 to 8).
P	Parity bit. Can be odd or even.
Sp	Stop bit, always high.
IDLE	No transfers on the communication line (RxDn or TxDn). An IDLE line must be high.

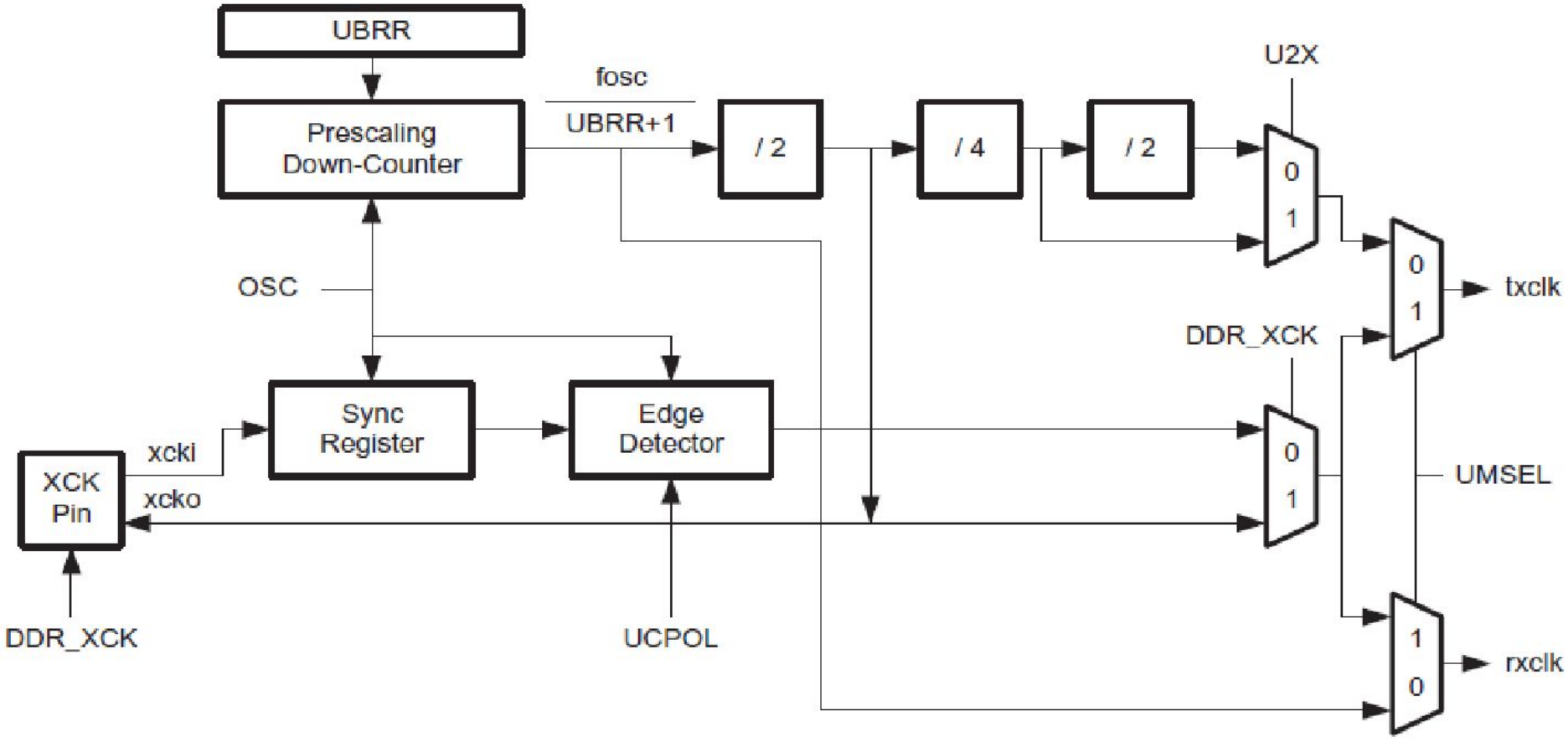
Pentru minimizarea riscul apariției erorilor – fiecare bit se eșantionează de 16 (8) ori, apoi se aplică funcția de vot majoritar.

Bit sampling



În modul "High Speed" (U2X=1) eșanționarea fiecărui bit se face de 8 ori.

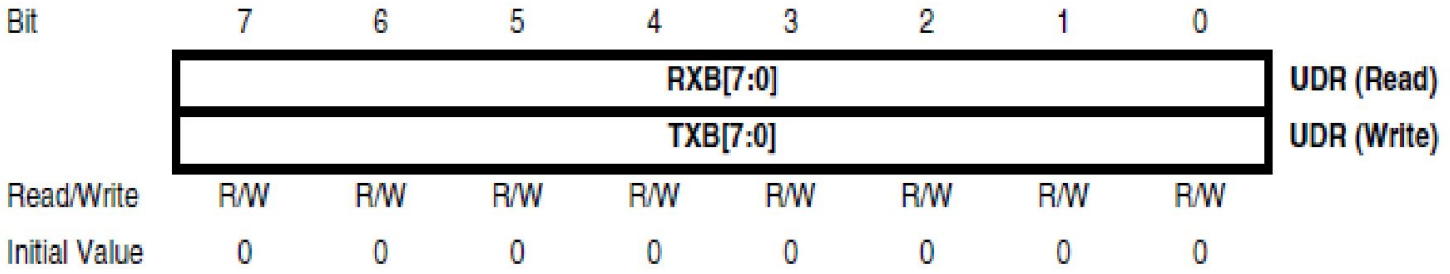
Generatorul de ceas



Operating Mode	Equation for Calculating Baud Rate[1]	Equation for Calculating UBRR Value
Asynchronous Normal Mode (U2X = 0)	$BAUD = \frac{f_{OSC}}{16(UBRR+1)}$	$UBRR = \frac{f_{OSC}}{16BAUD} - 1$
Asynchronous Double Speed Mode (U2X = 1)	$BAUD = \frac{f_{OSC}}{8(UBRR+1)}$	$UBRR = \frac{f_{OSC}}{8BAUD} - 1$
Synchronous Master Mode	$BAUD = \frac{f_{OSC}}{2(UBRR+1)}$	$UBRR = \frac{f_{OSC}}{2BAUD} - 1$

Registrul de date

USART I/O Data Register – UDR



Registrul receptorului este buferizat (*FIFO*).

Registrul de control

USART Control and Status Register A – UCSRA

Bit	7	6	5	4	3	2	1	0	
	RXC	TXC	UDRE	FE	DOR	PE	U2X	MPCM	UCSRA
Read/Write	R	R/W	R	R	R	R	R/W	R/W	
Initial Value	0	0	1	0	0	0	0	0	

- Bit 7 – RXC: USART Receive Complete
- Bit 6 – TXC: USART Transmit Complete
- Bit 5 – UDRE: USART Data Register Empty
- Bit 4 – FE: Frame Error
- Bit 3 – DOR: Data OverRun
- Bit 2 – PE: Parity Error
- Bit 1 – U2X: Double the USART Transmission Speed
- Bit 0 – MPCM: Multi-processor Communication Mode

Registrul de control

USART Control and Status Register B – UCSRB

Bit	7	6	5	4	3	2	1	0
	RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Initial Value	0	0	0	0	0	0	0	0

- Bit 7 – RXCIE: RX Complete Interrupt Enable
- Bit 6 – TXCIE: TX Complete Interrupt Enable
- Bit 5 – UDRIE: USART Data Register Empty Interrupt Enable
- Bit 4 – RXEN: Receiver Enable
- Bit 3 – TXEN: Transmitter Enable
- Bit 2 – UCSZ2: Character Size
- Bit 1 – RXB8: Receive Data Bit 8
- Bit 0 – TXB8: Transmit Data Bit 8

Registrul divizorului de ceas

USART Baud Rate Registers – UBRRL and UBRRH

Bit	15	14	13	12	11	10	9	8	
	URSEL	–	–	–	UBRR[11:8]				UBRRH
	UBRR[7:0]								UBRRL
	7	6	5	4	3	2	1	0	
Read/Write	R/W	R	R	R	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

!!! În unele MCU din seria AVR registrul UBRRH și UCSRC este mapat pe aceiași adresă. Selectarea între cele două se face prin intermediul bitului 7 de date.