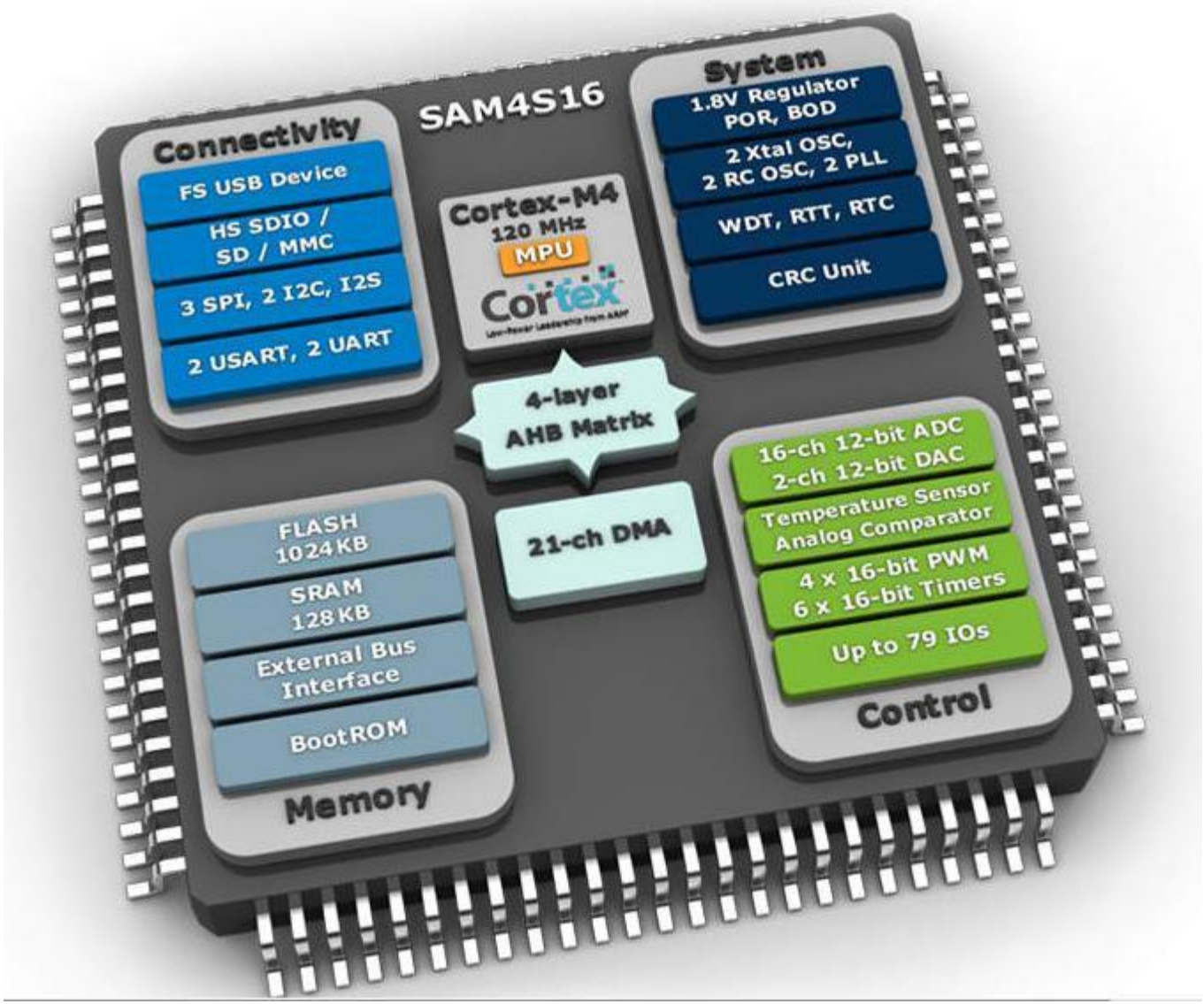
Nucleul ARM Cortex M

I. Clasificarea.
II. Blocul de regiștri.
III. Harta de memorie.

I. Procesoare ARM Cortex - M



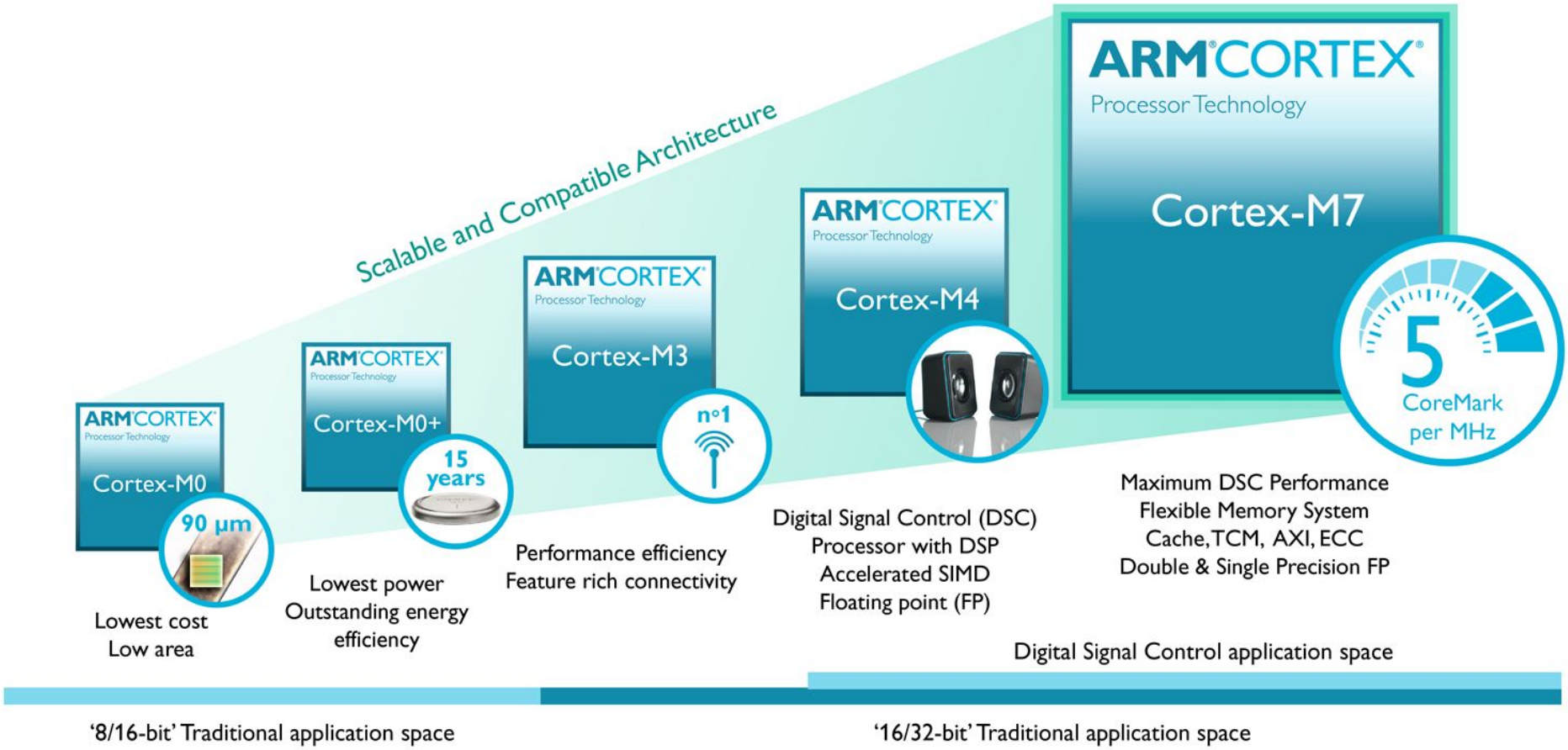
***Procesorul* Cortex-M face parte din familia de procesoare bazate pe arhitectura RISC ce este dezvoltată de *ARM Holdings*.**

Indexul "M" specifică ca acest procesor se utilizează în microcontrolere.

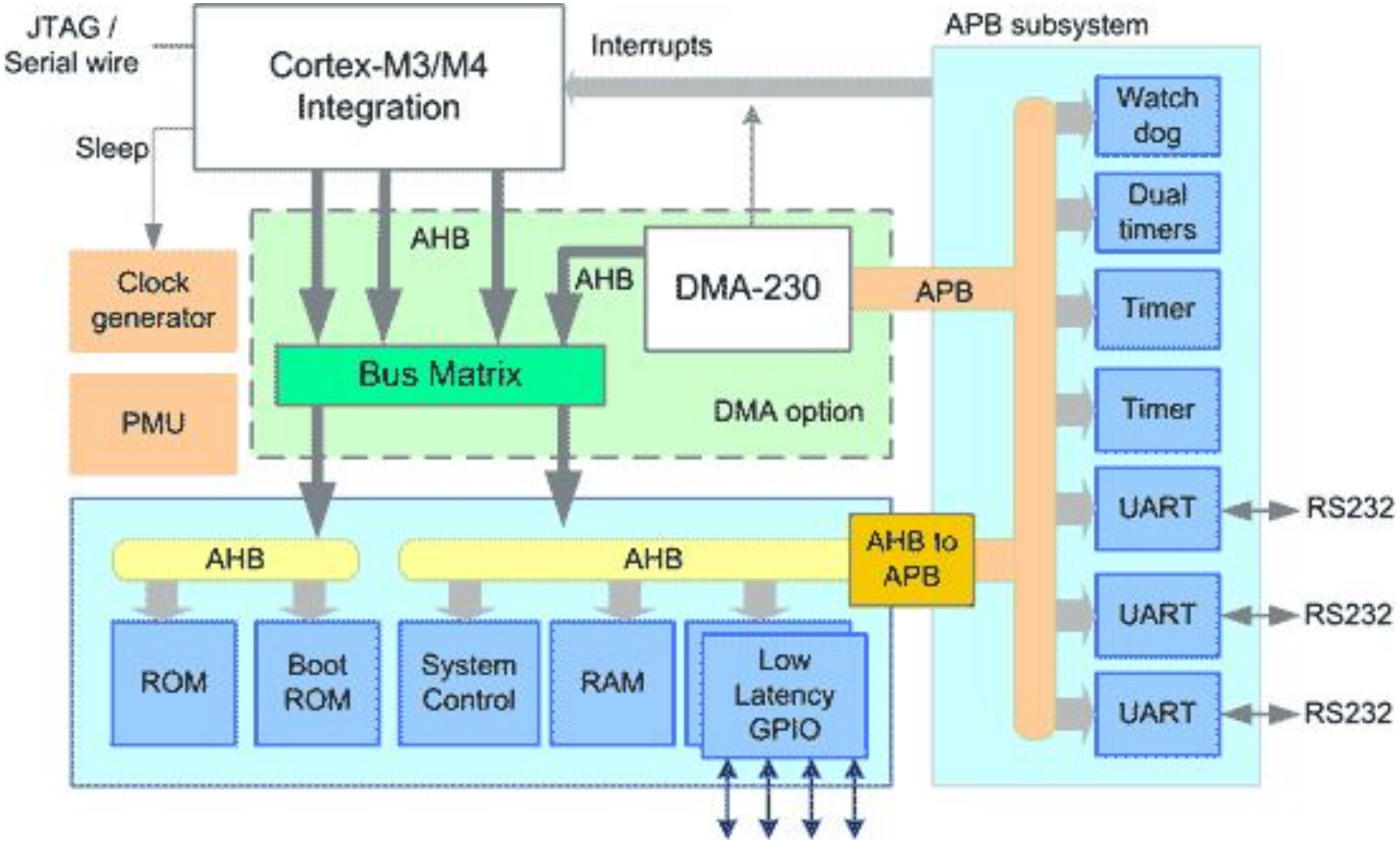
La moment sunt nomenclatura procesoarelor Cortex-M include următoarele procesoare: M0, M0+, M1, M3, M4, M7

Toate procesoarele *Cortex-M* suportă setul de instrucțiuni *Thumb-2*

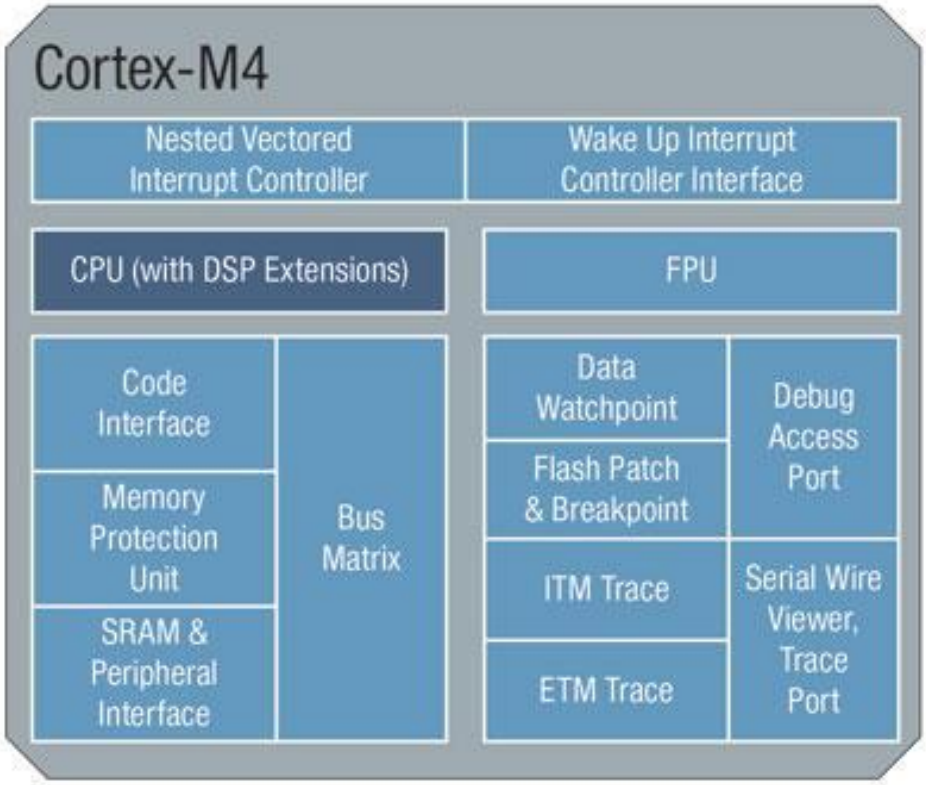
I. Structura nucleului ARM

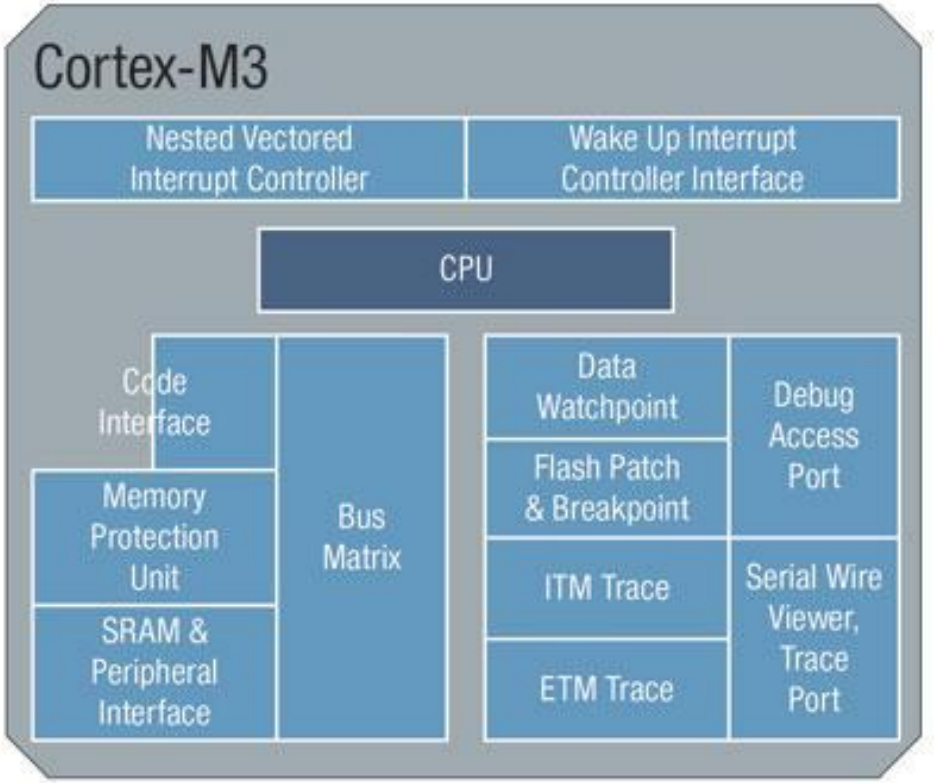


I. Structura nucleului ARM

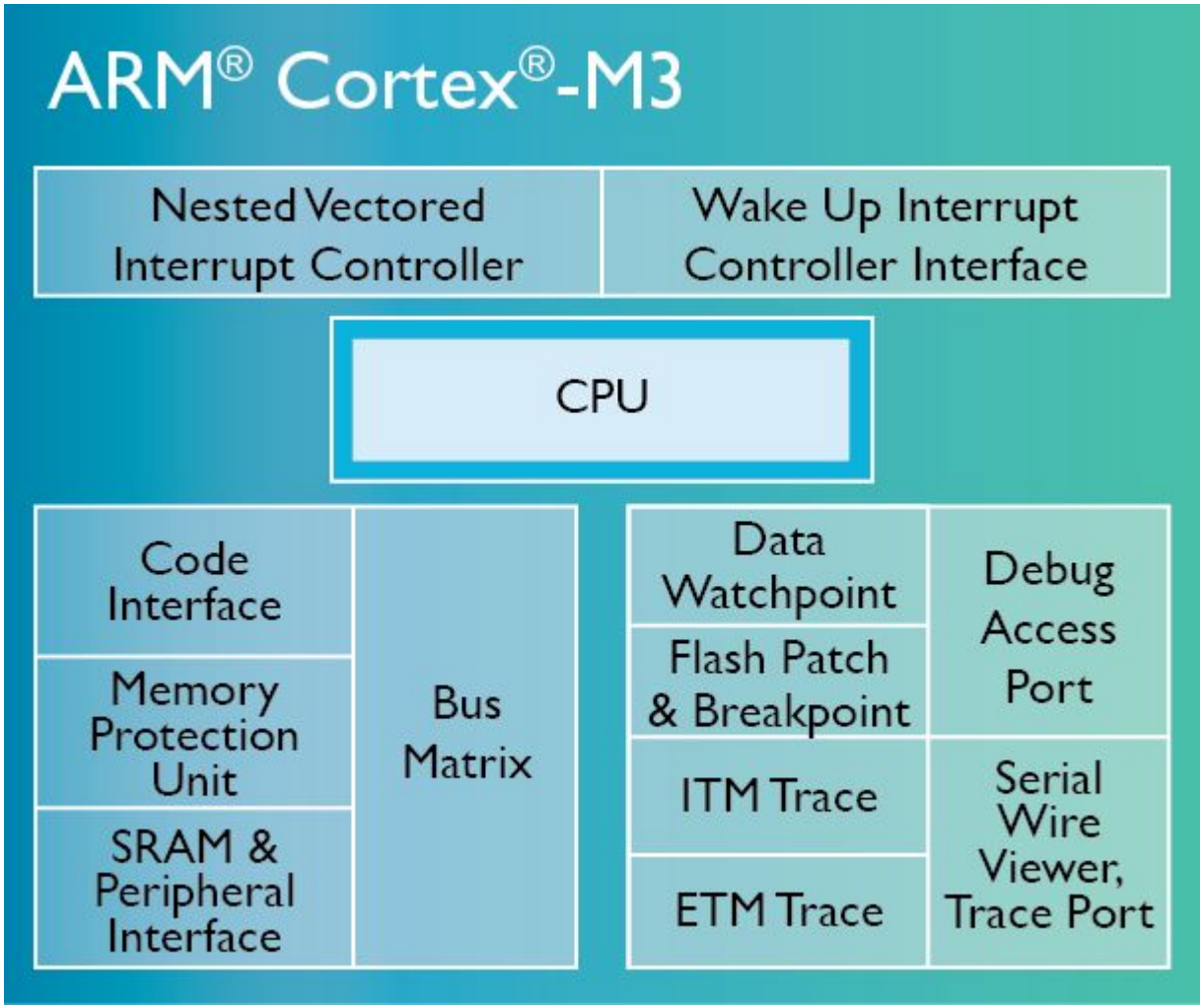


I. Structura nucleului ARM

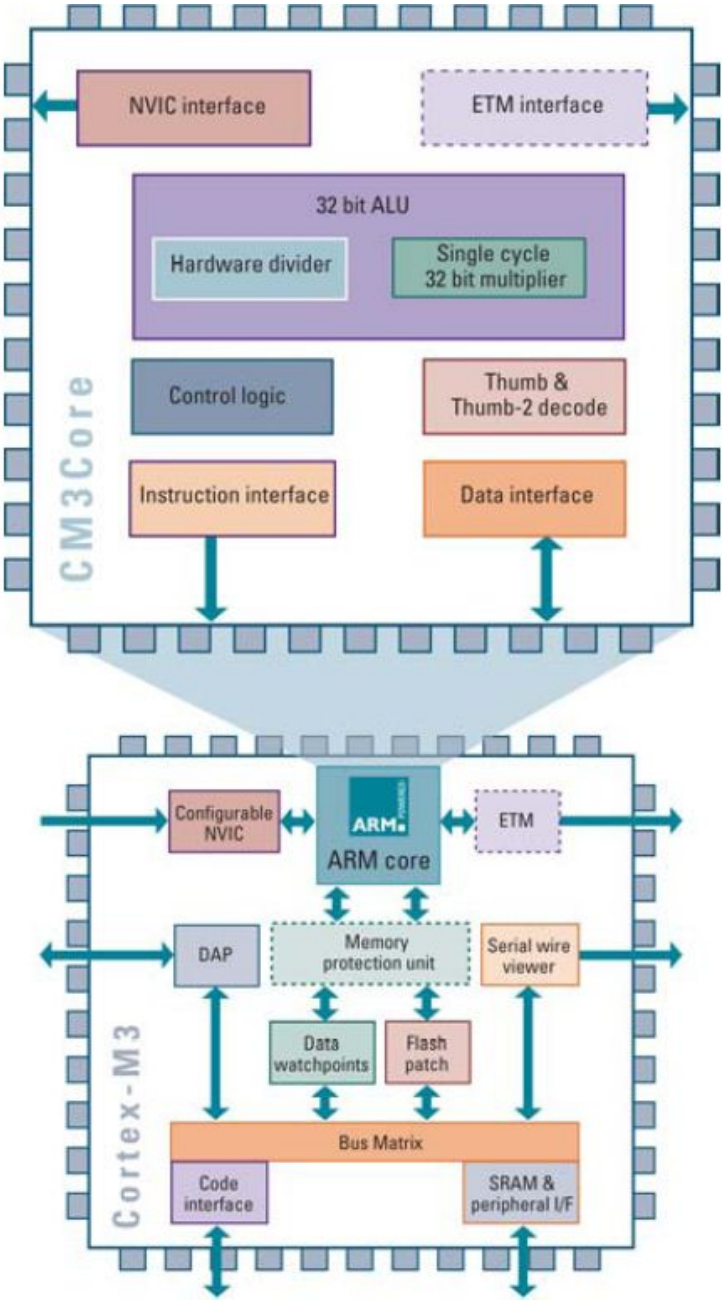




I. Structura nucleului ARM



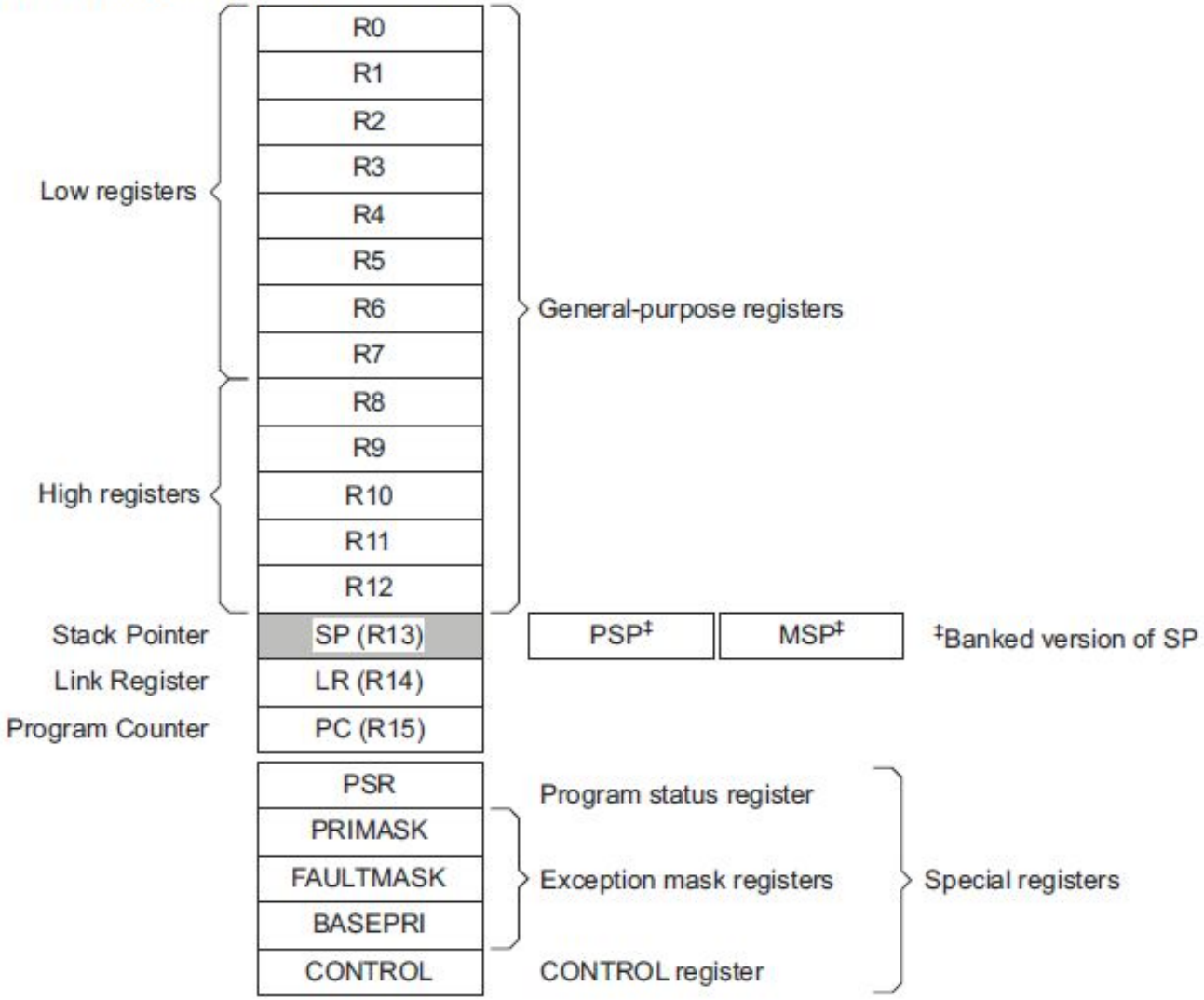
I. Structura microcontrolerului cu nucleul Cortex-M



- ***Arhitectura ARMv7-M***
- ***Setul de instrucțiuni Thumb și Thumb-2***
- ***Inmulțirea -1 cicluri, Inpărțirea -2..12 cicluri***
- ***Aritmetica cu saturație***
- ***Memorie*** Bit Banding
- ***Pipeline cu 3 nivele***
- ***Pîna la 240 vectori de intrerupere + NMI***
- ***256 nivele de prioritate a întreruperilor***
- ***Latența intrării in intrerupere 12 cicluri***

Core registers

The processor core registers are:

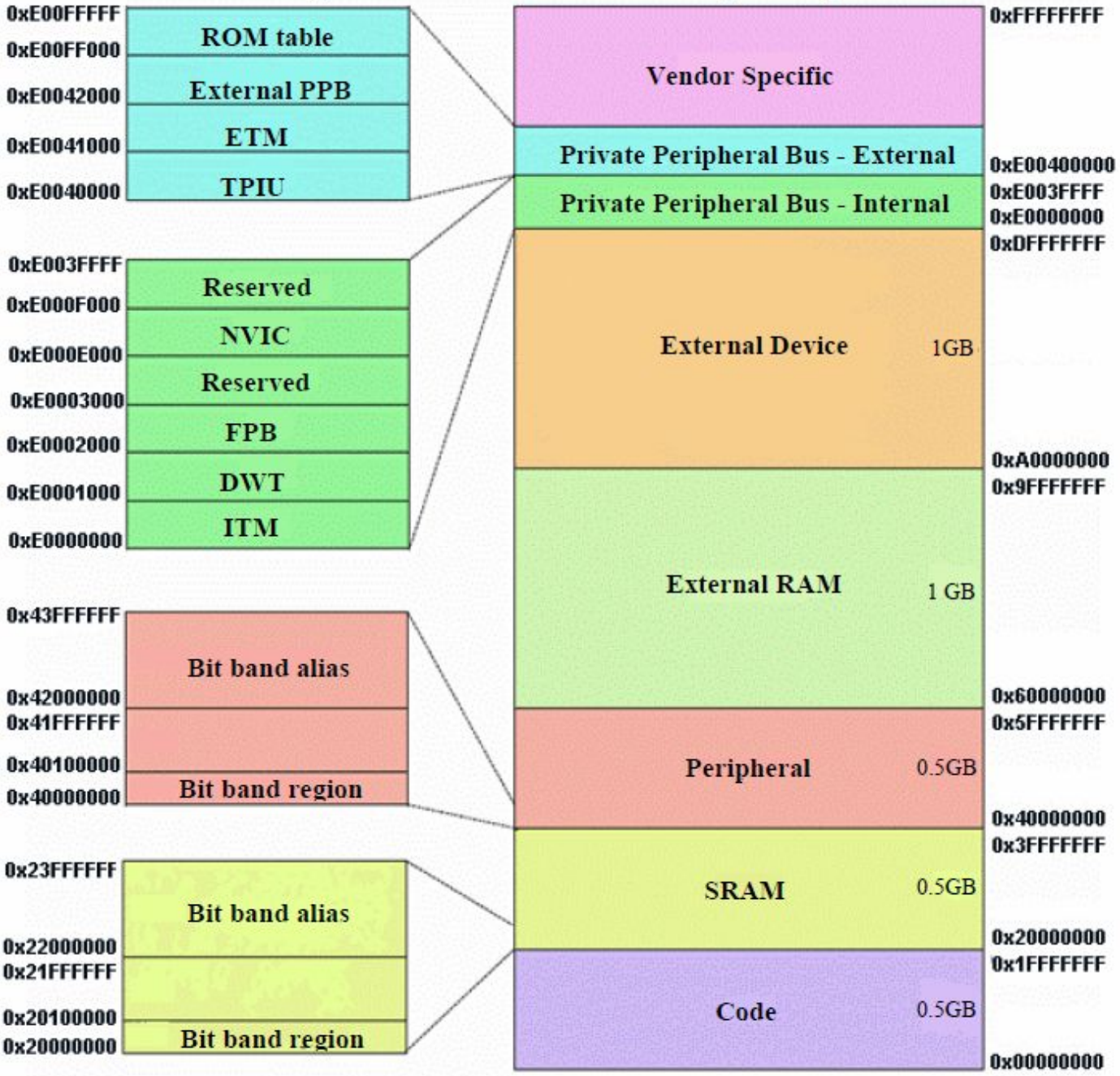


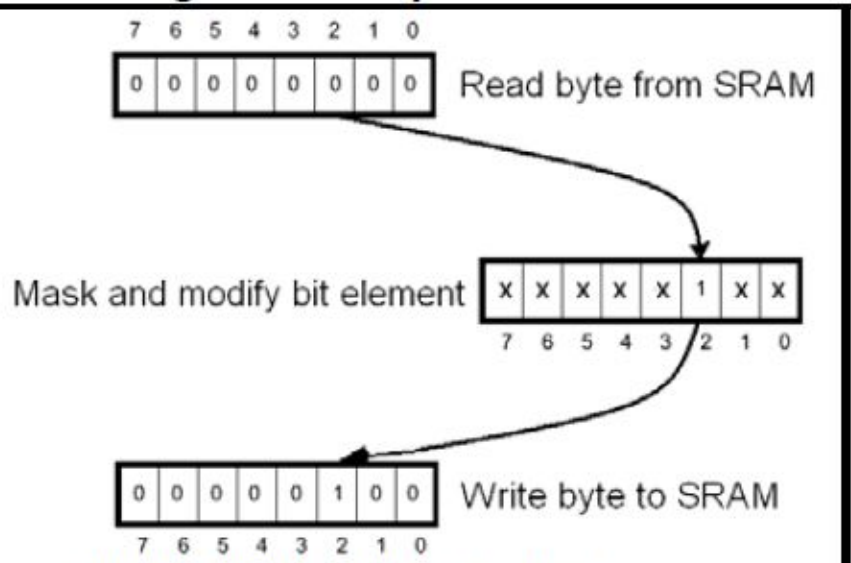
II. Blocul de registri

Name	Type (1)	Required privilege (2)	Reset value	Description
R0-R12	RW	Either	Unknown	"General-purpose registers" on page 43
MSP	RW	Privileged	See description	"Stack Pointer" on page 43
PSP	RW	Either	Unknown	"Stack Pointer" on page 43
LR	RW	Either	0xFFFFFFFF	"Link Register" on page 43
PC	RW	Either	See description	"Program Counter" on page 43
PSR	RW	Privileged	0x01000000	"Program Status Register" on page 44
ASPR	RW	Either	0x00000000	"Application Program Status Register" on page 45
IPSR	RO	Privileged	0x00000000	"Interrupt Program Status Register" on page 46
EPSR	RO	Privileged	0x01000000	"Execution Program Status Register" on page 46
PRIMASK	RW	Privileged	0x00000000	"Priority Mask Register" on page 47
FAULTMASK	RW	Privileged	0x00000000	"Fault Mask Register" on page 48
BASEPRI	RW	Privileged	0x00000000	"Base Priority Mask Register" on page 49
CONTROL	RW	Privileged	0x00000000	"CONTROL register" on page 50

1. Describes access type during program execution in thread mode and Handler mode. Debug access can differ.
2. An entry of Either means privileged and unprivileged software can access the register.

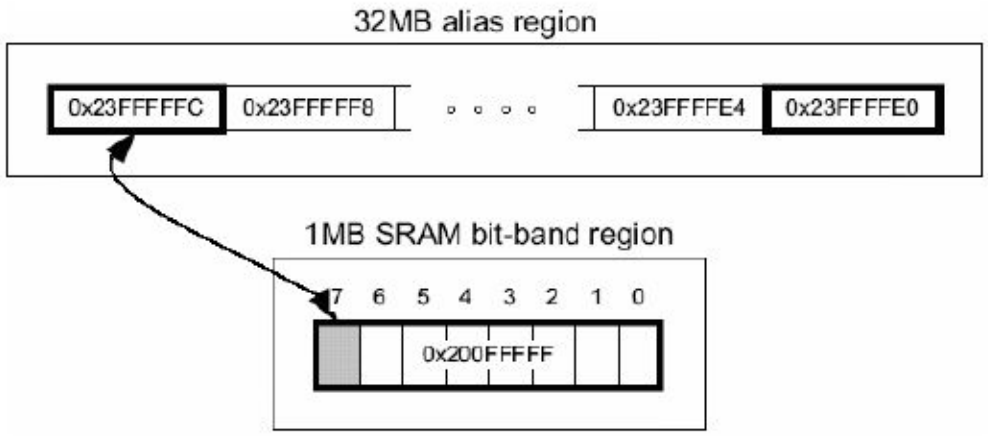
III. Harta de Memorie






```
LDR R0,=0x200FFFFF ; Setup address
MOV R2, #0x4       ; Setup data
LDR R1, [R0]       ; Read
ORR R1, R2         ; Modify bit
STR R1, [R0]       ; Write back result
```

Traditional bit manipulation method




```
LDR R0,=0x23FFFFFC ; Setup address
MOV R1, #0x1       ; Setup data
STR R1, [R0]       ; Write
```

Direct, single cycle access with bit banding

Structura controlerului TI DSP+CortexM