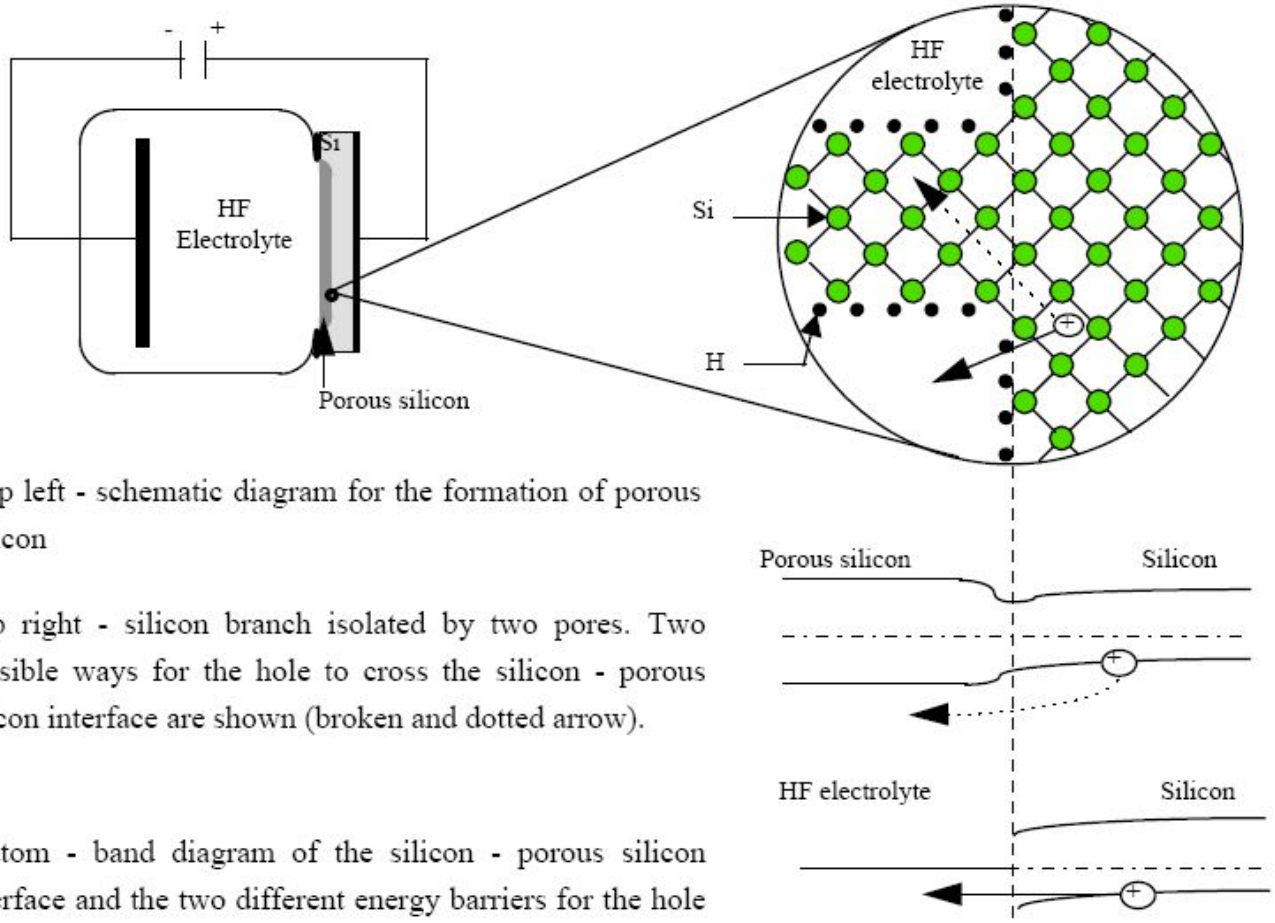
# Porous Silicon

- Porous Si is produced by room temperature electrochemical etching of Si in HF.
- If configured as an electrode in an HF-based electrochemical circuit, positive charge carriers (holes) at the Si surface facilitate the exchange of F atoms with H atoms, that terminate the Si surface.
- The exchange continues in the subsurface region, leading to the eventual removal of the fluorinated Si.
- The quality of the etched surface is related to the density of holes at the surface, which is controlled by the applied current density.

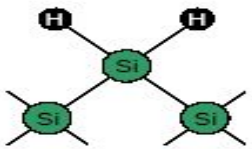



Top left - schematic diagram for the formation of porous silicon

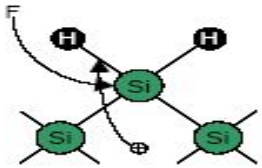
Top right - silicon branch isolated by two pores. Two possible ways for the hole to cross the silicon - porous silicon interface are shown (broken and dotted arrow).

Bottom - band diagram of the silicon - porous silicon interface and the two different energy barriers for the hole penetrating into the wall (broken arrow) or into the electolyte (solid arrow)

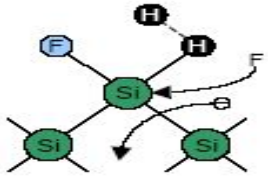
***Figure 2-6 Band diagram of the silicon - porous silicon interface where the radius of a silicon branch is small enough to exhibit quantum confinement (adapted from ref [24])***



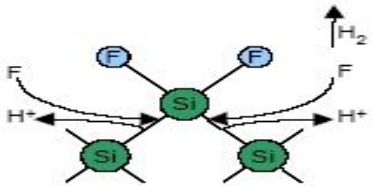

1. In the absence of electron holes, a hydrogen saturated silicon surface is virtually free from attack by flouride ions in the HF based electrolyte. The induced polarisation between the hydrogen and silicon atoms is low because the electron affinity of hydrogen is about that of silicon.



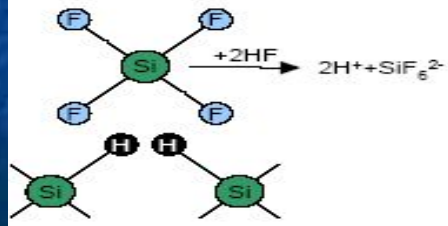

2. If a hole reaches the surface, nucleophillic attack on an Si-H bond by a fluoride ion can occur and a Si-F bond is formed.




3. The Si-F bond causes a polarisation effect allowing a second fluorine ion to attack and replace the remaining hydrogen bond. Two hydrogen atoms can then combine, injecting an electron into the substrate.




4. The polarisation induced by the Si-F bonds reduces the electron density of the remaining Si-Si backbonds making them susceptible to attack by the HF in a manner such that the remaining silicon surface atoms are bonded to the hydrogen atoms.




5. The silicon tretrafluoride molecule reacts with the HF to form the highly stable $SiF_6^{2-}$ fluoroanion.

The surface returns to its 'neutral' state until another hole is made available.

*Suggested mechanism for the electrochemical dissolution of silicon*

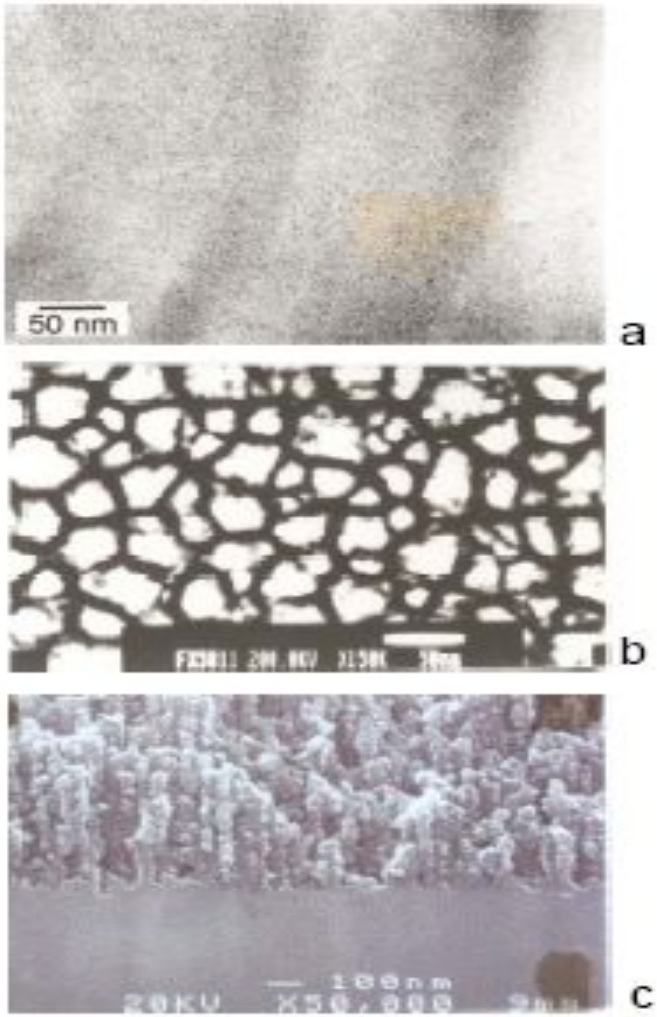



*Figure 2-8 Microstructure of porous silicon - a) Cross section of $p^-$ porous silicon (photograph taken from ref. [20]), b) Cross section of $p^+$ porous silicon (photograph supplied by Berger [27]), c) Planar view of $p^+$ porous silicon (photograph supplied by Loni [28])*

# FIPOS (full isolation by porous oxidised silicon)

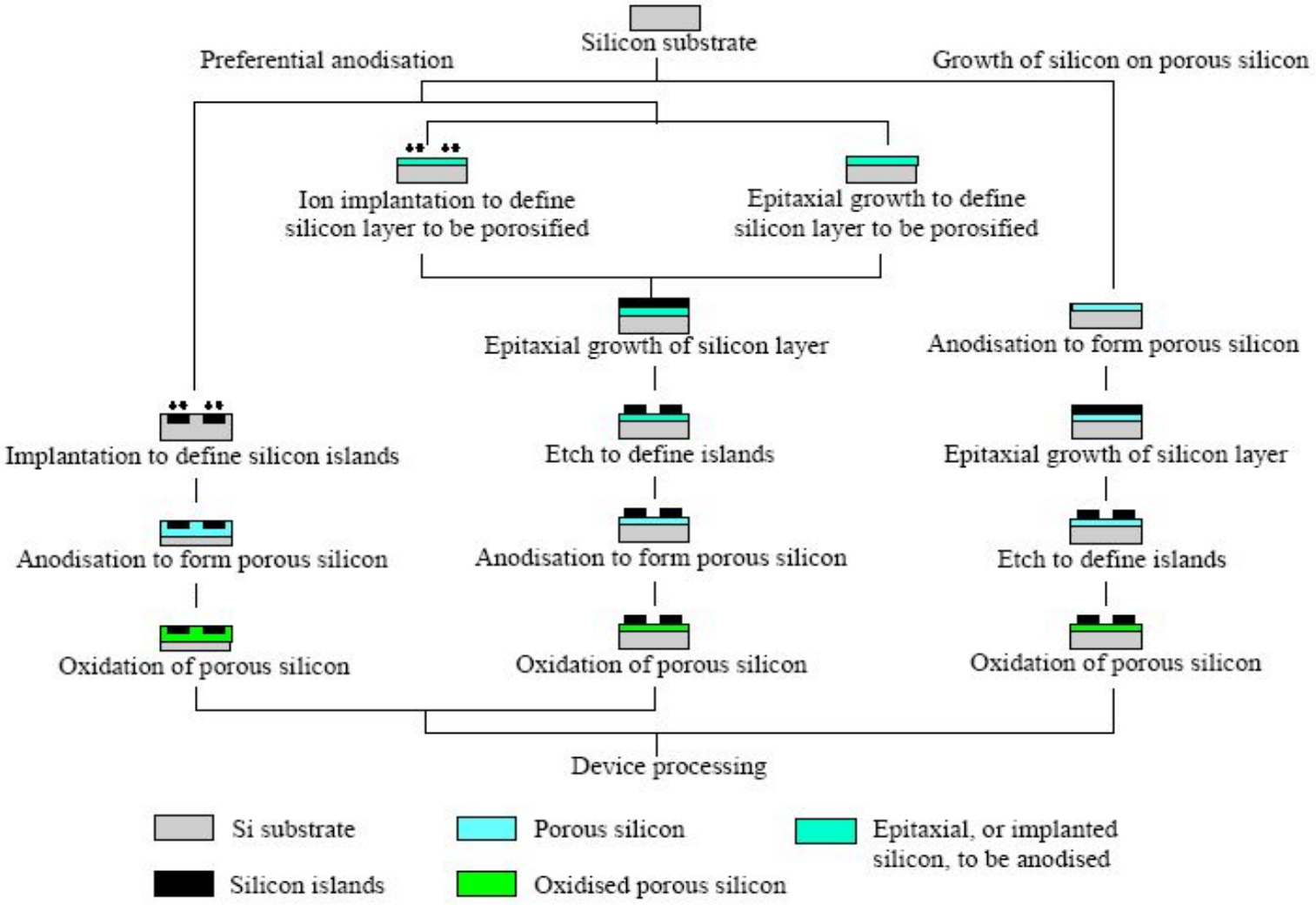



*Figure 2-9 Methods of implementing FIPOS technique*

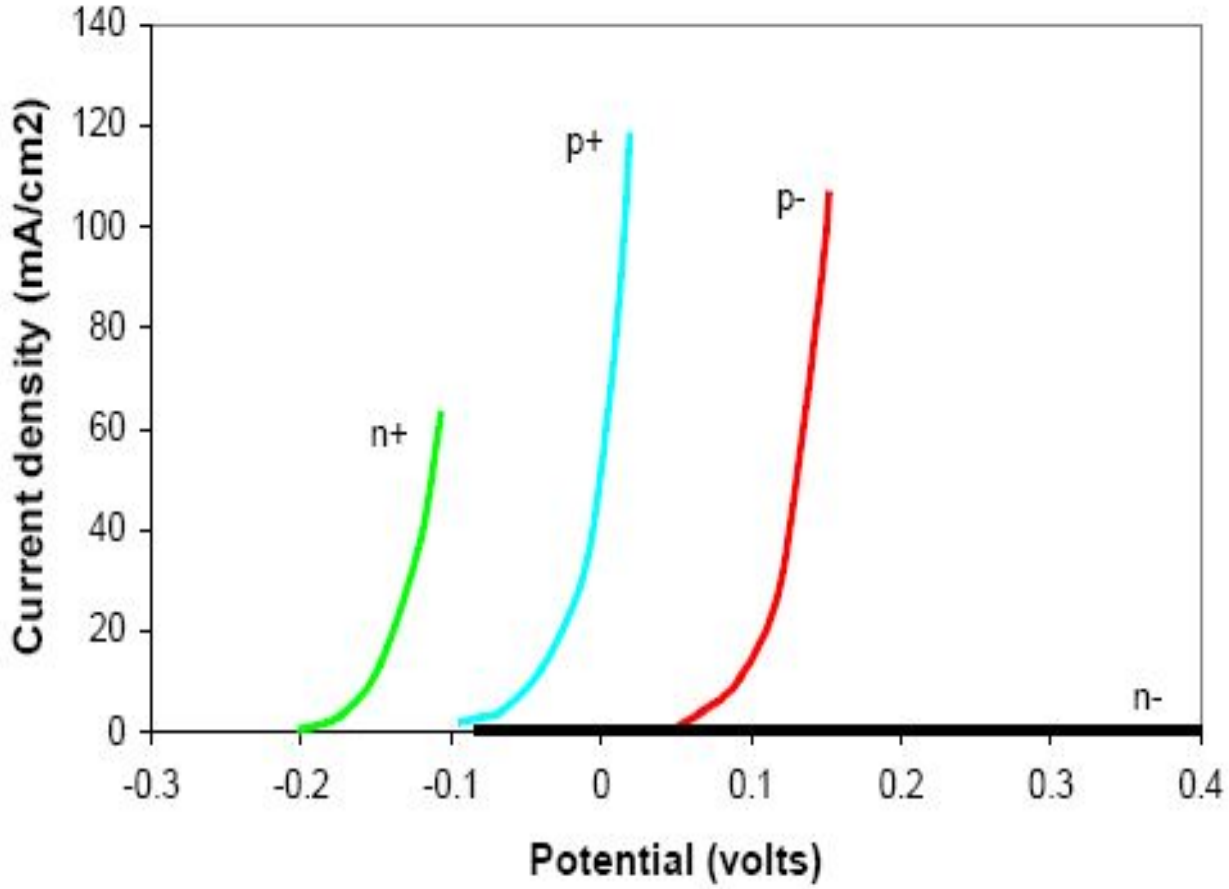



*Figure 2-10 Current density - potential graph for $p^+$, $p^-$, $n^+$ and $n^-$ silicon substrates (taken from ref [15])*

**Fundamentals of Porous Silicon PreparationFundamentals of Porous Silic**

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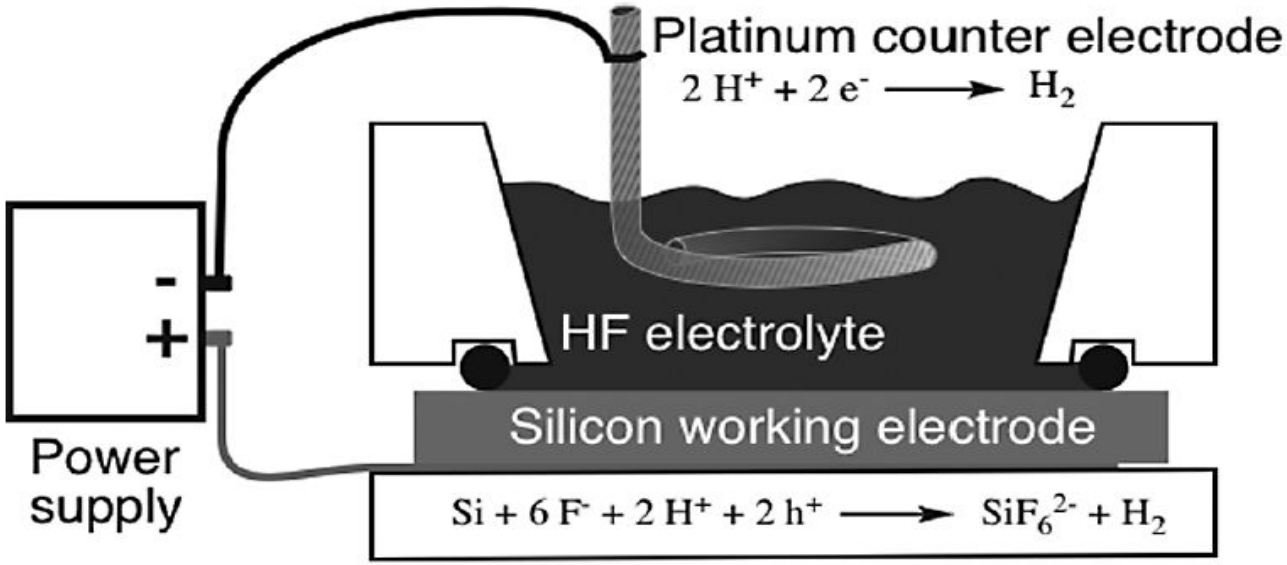



**Figure 1.2**
Schematic of a two-electrode electrochemical cell used to make porous silicon. Silicon is the working electrode. The working electrode is an anode in this case, because an oxidation reaction occurs at its surface. The cathode counter-electrode is typically platinum. The main oxidation and reduction half-reactions occurring during the formation of porous silicon are given.

- The techniques employed for dielectric isolation using porous silicon can also be used for micromachining applications.
- Micromachining is used to fabricate small-scale mechanical devices that are integrated with conventional microelectronics.
- Examples of micromachined devices include motors, cantilevers and a wide variety of sensors that are designed to sense temperature, IR and UV radiation, fluid flow or gas flow.
- Many of these structures are fabricated on free-standing membranes, structures that can be easily fabricated using porous silicon.

- For high current densities, the density of holes is high and the etched surface is smooth.
- For low current densities, the hole density is low and clustered in highly localized regions associated with surface defects.
- Surface defects become enlarged by etching, which leads to the formation of pores.
- Pore size and density are related to the type of Si used and the conditions of the electrochemical cell.
- Both single crystal and polycrystalline Si can be converted to porous Si.

- The large surface-to-volume ratios make porous Si attractive for gaseous and liquid applications, including filter membranes and absorbing layers for chemical and mass sensing.
- When single crystal substrates are used, the unetched porous layer remains single crystalline and is suitable for epitaxial Si growth.
- CVD coatings do not generally penetrate the porous regions, but rather overcoat the pores at the surface of the substrate.
- The formation of localized Si-on-insulator structures is possible by combining pore formation with epitaxial growth, followed by dry etching to create access (доступ) holes to the porous region, and thermal oxidation of the underlying porous region.

- A third application uses porous Si as a sacrificial layer for polysilicon and single crystalline Si surface micromachining.
- As shown by *Lang* et al., the process involves the electrical isolation of the solid structural Si layer by either p-n-junction formation through selective doping, or use of electrically insulating thin films, since the formation of pores only occurs on electrically charged surfaces.
- A weak Si etchant will aggressively attack the porous regions with little damage to the structural Si layers and can be used to release the devices.

# Silicon Dioxide

- Silicon dioxide ($SiO_2$) is one of the most widely used materials in the fabrication of MEMS.
- In polysilicon surface micromachining, $SiO_2$ is used as a sacrificial material, since it can be easily dissolved using etchants that do not attack polysilicon.
- $SiO_2$ is widely used as etch mask for dry etching of thick polysilicon films, since it is chemically resistant to dry etching processes for polysilicon.
- $SiO_2$ films are also used as passivation layers on the surfaces of environmentally sensitive devices.

- The most common processes used to produce $SiO_2$ films for polysilicon surface micromachining are thermal oxidation and LPCVD.
- Thermal oxidation of Si is performed at temperatures of 900 °C to 1,200 °C in the presence of oxygen or steam.
- Since thermal oxidation is a self-limiting process, the maximum practical film thickness that can be obtained is about 2μm, which is sufficient for many sacrificial applications.
- Thermal oxidation of Si can only be performed on Si surfaces.

- $SiO_2$ films can be deposited on a wide variety of substrate materials by LPCVD.
- LPCVD provides a means for depositing thick (> 2μm) $SiO_2$ films at temperatures much lower than thermal oxidation.
- Known as low-temperature oxides (LTO), these films have a higher etch rate in HF than thermal oxides, which translates to significantly faster release times when LTO films are used as sacrificial layers.

- Phosphosilicate glass (PSG) can be formed using nearly the same deposition process as LTO by adding a phosphorus-containing gas to the precursor flows.

- PSG films are useful as sacrificial layers, since they generally have higher etching rates in HF than LTO films

- PSG and LTO films are deposited in hot-wall, low pressure, fused silica furnaces in systems similar to those described previously for polysilicon.

- Precursor gases include $SiH_4$ as a Si source, $O_2$ as an oxygen source, and, in the case of PSG, $PH_3$ as a source of phosphorus.

- LTO and PSG films are typically deposited at temperatures of 425 °C to 450 °C and pressures ranging from 200 mtorr to 400 mtorr.

- The low deposition temperatures result in LTO and PSG films that are slightly less dense than thermal oxides, due to the incorporation of hydrogen in the films.
- LTO films can, however, be densified by an annealing step at high temperature (1,000 ˚C).
- The low density of LTO and PSG films is partially responsible for the increased etch rate in HF.

- Thermal $SiO_2$ and LTO are electrical insulators used in numerous MEMS applications.
- The dielectric constants of thermal oxide and LTO are 3.9 and 4.3, respectively.
- The dielectric strength of thermal $SiO_2$ is $1.1 \cdot 10^6$ V/cm, and for LTO it is about 80% of that value.
- The stress in thermal $SiO_2$ is compressive with a magnitude of about 300 MPa.

- For LTO the as-deposited residual stress is tensile, with a magnitude of about 100 MPa to 400 MPa.
- The addition of phosphorous to LTO decreases the tensile residual stress to about 10 MPa for phosphorus concentrations of 8% .
- As with polysilicon, the properties of LTO and PSG are dependent on processing conditions.

- Plasma-enhanced chemical vapor deposition (PECVD) is another common method to produce oxides of silicon.
- Using a plasma to dissociate the gaseous precursors, the deposition temperatures needed to deposit PECVD oxide films is lower than for LPCVD films.
- For this reason, PECVD oxides are quite commonly used as masking, passivation, and protective layers, especially on devices that have been coated with metals.

- Quartz is the crystalline form of $SiO_2$ and has interesting properties for MEMS.
- Quartz is optically transparent, piezoelectric, and electrically insulating.
- Like single crystal Si, quartz substrates are available as high quality, large area wafers that can be bulk micromachined using anisotropic etchants.
- Quartz has recently become a popular substrate material for microfluidic devices due to its optical, electronic, and chemical properties.

- Another $SiO_2$-related material that has recently found uses in MEMS is spin-on-glass (SOG).

- SOG is a polymeric material with a viscosity suitable for spin coating. Two recent publications illustrate the potential for SOG in MEMS fabrication.

- In the first example, *Yasseen* et al. detailed the development of SOG as a thick-film sacrificial molding material for thick polysilicon films. The authors reported a process to deposit, polish, and etch SOG films that were 20 microns thick.

- The thick SOG films were patterned into molds and filled with 10 micron-thick LPCVD polysilicon films, planarized by selective CMP, and subsequently dissolved in a wet etchant containing HCl, HF, and $H_2O$ to reveal (обнажить) the patterned polysilicon structures.

- The cured (отвержденная) SOG films were completely compatible with the polysilicon deposition process.

- In the second example, *Liu* et al. fabricated high-aspect ratio channel plate microstructures from SOG.
- Electroplated nickel (Ni) was used as a molding material, with Ni channel plate molds fabricated using a conventional LIGA process.
- The Ni molds were then filled with SOG, and the sacrificial Ni molds were removed in a reverse electroplating process.
- In this case, the fabricated SOG structures (over 100 microns tall) were micromachined glass structures fabricated using a molding material more commonly used for structural components.

- Thick (5–100 μm) spin-on glass (SOG) has the ability to uniformly coat surfaces and smooth out underlying topographical variations, effectively planarizing surface features.

- Thin (0.1–0.5 μm) SOG was heavily investigated in the integrated circuit industry as an interlayer dielectric between metals for high-speed electrical interconnects; however, its electrical properties are considered poor compared to thermal or CVD silicon oxides.

- Spin-on glass is commercially available in different forms, commonly ***siloxane- or silicate-based.*** The latter type allows water absorption into the film, resulting in a higher relative dielectric constant and a tendency to crack.

- After deposition, the layer is typically densified at a temperature between 300º and 500ºC.

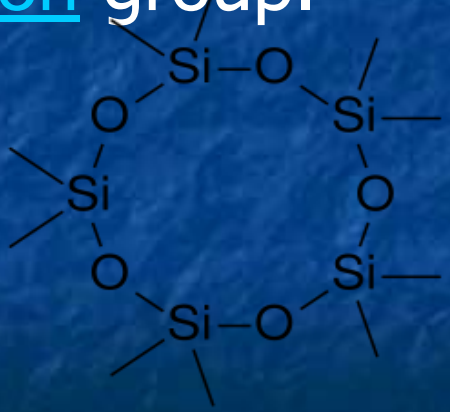
- Measured film stress is approximately 200 MPa in tension but decreases substantially with increasing anneal temperatures.

There are two basic types of ***SOG***: ***siloxane-based organic SOG*** and ***silicate-based*** inorganic ***SOG***.

- Spin on glass (SOG) is a mixture of $SiO_2$ and dopants (either boron or phosphorous) that is suspended in a solvent solution.
- The SOG is applied to a clean silicon wafer by spin-coating just like photoresist.

# A **siloxane**

- A **siloxane** is any chemical compound composed of units of the form $R_2SiSiOSiO$, where R is a hydrogenSiO, where R is a hydrogen atom or a hydrocarbon group.



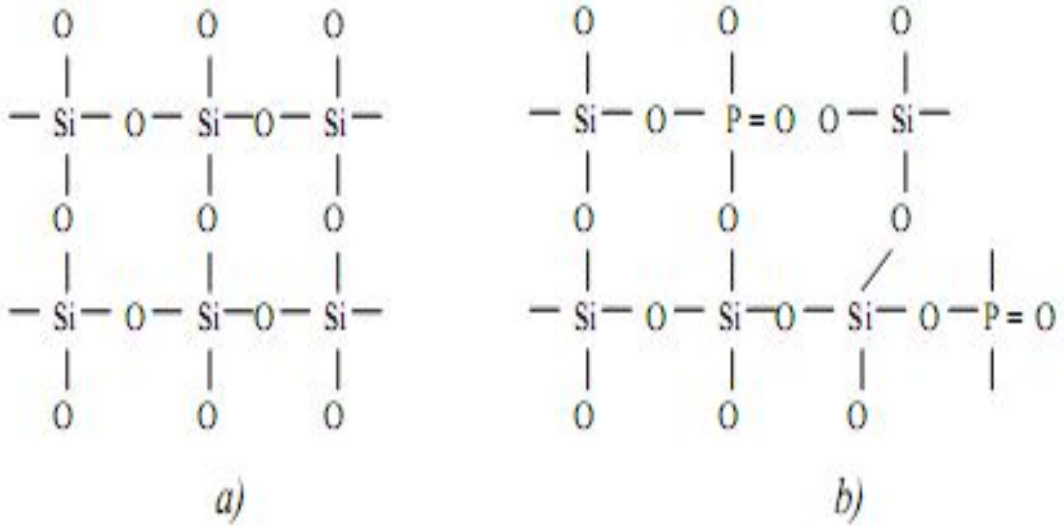
| Cyclic siloxanes | Linear siloxanes |
| --- | --- |
| D3: hexamethylcyclotrisiloxane | MM: hexamethyldisiloxane |
| D4: octamethylcyclotetrasiloxane | MDM: octamethyltrisiloxane |
| D5: decamethylcyclopentasiloxane | MD2M: decamethyltetrasiloxane |
| D6: dodecamethylcyclohexasiloxane | MDnM: polydimethylsiloxane |

**An examples are: $[SiO(CH_3)_2]_n$ (polydimethylsiloxane) and $[SiO(C_6H_5)_2]_n$ (polydiphenylsiloxane).**

# Silicate-based SOG

### 1.3.1. Silicate based compounds

The silicate SOG is formed from a condensation reaction of $Si(OH)_4$ by losing water. When the film is fully cured, the film should form a strong Si-O network and contain no -OH but it has fairly significant shrinkage. A rough description of the molecular structure [1] is presented in the following figure:



*a)* *b)*

*Figure 1-2: a) Silicate SOG and b) P-doped silicate SOG*

# Silicon Nitride

- Silicon nitride ($Si_3N_4$) is widely used in MEMS for electrical isolation, surface passivation, etch masking, and as a mechanical material.
- Two deposition methods are commonly used to deposit $Si_3N_4$ thin films: LPCVD and PECVD.
- .

- PECVD silicon nitride is generally nonstoichiometric (sometimes denoted as $Si_xN_y$ : H) and may contain significant concentrations of hydrogen.

- Use of PECVD silicon nitride in micromachining applications is somewhat limited because it has a high etch rate in HF (e.g., often higher than that of thermally grown $SiO_2$).

- However, PECVD offers the ability to deposit nearly stress-free silicon nitride films, an attractive property for encapsulation and packaging.

- Unlike its PECVD counterpart, LPCVD $Si_3N_4$ is extremely resistant to chemical attack, making it the material of choice for many Si bulk and surface micromachining applications.

- LPCVD $Si_3N_4$ is commonly used as an insulating layer because it has a resistivity of $10^{16}\ \Omega \cdot cm$ and field breakdown limit of $10^7$ V/cm.

- LPCVD $Si_3N_4$ films are deposited in horizontal furnaces similar to those used for polysilicon deposition.

- Typical deposition temperatures and pressures range between 700 °C to 900 °C and 200 mtorr to 500 mtorr, respectively.

- The standard source gases are dichlorosilane ($SiH_2Cl_2$) and ammonia ($NH_3$), to produce stoichiometric $Si_3N_4$, a $NH_3$ to $SiH_2Cl_2$ ratio of 10:1 is commonly used.

- The microstructure of films deposited under these conditions is amorphous.

- The residual stress in stoichiometric $Si_3N_4$ is large and tensile, with a magnitude of about 1GPa.
- Such a large residual stress causes films thicker than a few thousand angstroms to crack.
- Nonetheless, thin stoichiometric $Si_3N_4$ films have been used as mechanical support structures and electrical insulating layers in piezoresistive pressure sensors

- **Стехиометрия** (от др.-греч. (от др.-греч. στοιχεῖον «элемент» + μετρέω «измерять») — раздел химии (от др.-греч. στοιχεῖον «элемент» + μετρέω «измерять») — раздел химии о соотношениях реагентов в химических реакциях.

- Позволяет теоретически вычислять необходимые массы и объёмы реагентов.

- Отношения количеств реагентов, равные отношениям коэффицентов в стехиометрическом уравненииОтношения количеств реагентов, равные отношениям коэффицентов в стехиометрическом уравнении реакции, называются *стехиометрическими*. Если вещества реагируют в соотношении 1:1, то их соответственные количества называют *эквимолярными*.

- Рассмотрим реакцию термитной смеси:
  - $Fe_2O_3 + 2Al \rightarrow Al_2O_3 + 2Fe$.
- Сколько граммов алюминия нам необходимо для завершения реакции с 85.0 граммами оксида оксида железа (III)?

$$m_{Al} = \left(\frac{85.0\ g\ Fe_2O_3}{1}\right)\left(\frac{1\ mol\ Fe_2O_3}{159.7\ g\ Fe_2O_3}\right)\left(\frac{2\ mol\ Al}{1\ mol\ Fe_2O_3}\right)\left(\frac{27.0\ g\ Al}{1\ mol\ Al}\right) = 28.7\ g$$

- Таким образом, для проведения реакции с 85.0 граммами оксидаТаким образом, для проведения реакции с 85.0 граммами оксида железаТаким образом, для проведения реакции с 85.0 граммами оксида железа (III), необходимо 28.7 граммов алюминия.

- To enable the use of $Si_3N_4$ films for applications that require micron thick, durable (прочные), and chemically resistant membranes, $Si_xN_y$ films can be deposited by LPCVD.

- These films, often referred to as Si-rich or low-stress nitride, are intentionally deposited with an excess of Si by simply decreasing the ratio of $NH_3$ to $SiH_2Cl_2$ during deposition.

- Nearly stress-free films can be deposited using a $NH_3$ to $SiH_2Cl_2$ ratio of 1 : 6, a deposition temperature of 850 °C, and a pressure of 500 mtorr.
- The increase in Si content not only leads to a reduction in tensile stress, but also a decrease in the etch rate in HF.
- Such properties have enabled the development of fabrication techniques that would otherwise not be feasible with stoichiometric $Si_3N_4$.

# Germanium-Based Materials

- Like Si, Ge has a long history as a semiconductor device material, dating back to the development of the earliest transistors and semiconductor strain gauges.
- Issues related to the water solubility of germanium oxide, however, stymied the development of Ge for microelectronic devices.
- Nonetheless, there is a renewed interest in using Ge in micromachined devices due to the relatively low processing temperatures required to deposit the material.

# Polycrystalline Ge

- Thin polycrystalline Ge (poly-Ge) films can be deposited by LPCVD at temperatures as low as 325 °C on Si, Ge, and SiGe substrates.

- Ge does not nucleate on $SiO_2$ surfaces, which prohibits the use of thermal oxides and LTO films as sacrificial layers, but enables the use of these films as sacrificial molds.

- Residual stress in poly-Ge films deposited on Si substrates can be reduced to nearly zero after short anneals at modest temperatures (30 s at 600 °C).

- Poly-Ge is essentially impervious (невосприимчивый) to KOH, TMAH, and BOE, enabling the fabrication of Ge membranes on Si substrates.

- The mechanical properties of poly-Ge are comparable to polysilicon, having a Young's modulus of 132 GPa and a fracture stress between 1.5 GPa and 3.0 GPa.

- Mixtures of $HNO_3$, $H_2O$, and HCl and $H_2O$, $H_2O_2$, and HCl, as well as the RCA SC-1 cleaning solution isotropically etch Ge.

- Since these mixtures do not etch Si, $SiO_2$, $Si_3N_4$, and SiN, poly-Ge can be used as a sacrificial substrate layer in polysilicon surface micromachining.

- RCA, the Radio Corporation of America

- Werner KernWerner Kern developed the basic procedure in 1965 while working for RCA, the Radio Corporation of America. It involves the following :

- 1. Removal of the organic contaminants (Organic Clean)

- 2. Removal of thin oxide layer (Oxide Strip)

- 3. Removal of ionic contamination (Ionic Clean)

- The wafers are prepared by soaking them in DI waterThe wafers are prepared by soaking them in DI water. The first step (called SC-1, where SC stands for Standard Clean) is performed with a 1:1:5 solution of $NH_4OH$ (ammonium hydroxide) + $H_2O_2$ (hydrogen peroxide) + $H_2O$ (water) at 75 or 80 °C typically for 10 minutes.

- This treatment results in the formation of a thin silicon dioxideThis treatment results in the formation of a thin silicon dioxide layer (about 10 Angstrom) on the silicon surface, along with a certain degree of metallic contamination (notably IronThis treatment results in the formation of a thin silicon dioxide layer (about 10 Angstrom) on the silicon surface, along with a certain degree of metallic contamination (notably Iron) that shall be removed in subsequent steps. This is followed by transferring the wafers into a DI water bath.

- The second step is a short immersion in a 1:50 solution of HF + $H_2O$ at 25 °C, in order to remove the thin oxide layer and some fraction of ionic contaminants.

- The third and last step (called SC-2) is performed with a 1:1:6 solution of HCl + $H_2O_2$ + $H_2O$ at 75 or 80 °C. This treatment effectively removes the remaining traces of metallic (ionic) contaminants.

- Using these techniques, devices such as poly-Ge-based thermistors and $Si_3N_4$ membrane-based pressure sensors, made using poly-Ge sacrificial layers, have been fabricated.

- *Franke* et al. found no performance degradation in Si CMOS devices following the fabrication of surface micromachined poly-Ge structures, thus demonstrating the potential for on-chip-integration of Ge electromechanical devices with Si circuitry.

# Polycrystalline SiGe

- Like poly-Ge, polycrystalline SiGe (poly-SiGe) is a material that can be deposited at temperatures lower than those required for polysilicon.
- Deposition processes include LPCVD, APCVD, and RTCVD (rapid thermal CVD) using $SiH_4$ and $GeH_4$ as precursor gases.
- Deposition temperatures range from 450 °C for LPCVD to 625 °C by rapid thermal CVD (RTCVD).

- In general, the deposition temperature is related to the concentration of Ge in the films, with higher Ge concentrations resulting in lower deposition temperatures.

- *Быстродействующее термическое химическое парофазное осаждение* (англ. *Rapid thermal CVD (RTCVD)*) — CVD-процесс, использующий лампы накаливания или другие методы быстрого нагрева подложки. Нагрев подложки без разогрева газа позволяет сократить нежелательные реакции в газовой фазе.

# rapid thermal oxidation (RTO)

Sundar Ramamurthy (2004). Solid State Technology

- RTO – one of **RTP** (rapid thermal processing)
- ambient to 1300°C
- ramp rate: 1°C/s to 300°C/s
- purge gas
- atmospheric or vacuum processing
- dry oxygen
- pyrometer control: 150°C - 1300°C
- applications:
  - sacrificial oxide
  - liner oxide (тонкое окисление) in STI
- typical growth rate 3 Å/s at 1150 °C
- tungsten-halogen lamps or Xe,Kr arc lamps
- multizone heater for uniform $T$
- $T$ variations < 2 °C

- Like polysilicon, poly-SiGe can be doped with boron and phosphorus to modify its conductivity.
- In situ boron doping can be performed at temperatures as low as 450 ◦C.
- *Sedky* et al. showed that the deposition temperature of conductive films doped with boron could be further reduced to 400 ◦C if the Ge content was kept at or above 70%.

- Unlike poly-Ge, poly-SiGe can be deposited on a number of sacrificial substrates, including $SiO_2$, PSG, and poly-Ge.

- For Ge rich films, a thin polysilicon seed layer is sometimes used on $SiO_2$ surfaces since Ge does not readily nucleate on oxide surfaces.

- Like many compound materials, variations in film composition can change the physical properties of the material.

- For instance, etching of poly-SiGe by $H_2O_2$ becomes significant for Ge concentrations over 70%.

- *Sedky* et al. have shown that the microstructure, film conductivity, residual-stress, and residual stress gradient are related to the concentration of Ge in the material.

- With respect to residual stress, *Franke* et al. produced in situ boron doped films with residual compressive stresses as low as 10 MPa.

- The poly-SiGe, poly-Ge material system is particularly attractive for surface micromachining since $H_2O_2$ can be used as a release agent.
- It has been reported that poly-Ge etches at a rate of 0.4microns/min in $H_2O_2$, while poly-SiGe with Ge concentrations below 80% have no observable etch rate after 40 hrs.
- The ability to use $H_2O_2$ as a sacrificial etchant makes the combination of poly-SiGe and poly-Ge extremely attractive for surface micromachining from the processing, safety, and materials compatibility points of view.

- Due to the conformal nature of LPCVD processing, poly-SiGe structural elements, such as gimbal-based microactuator (микроактюатор с кардановым подвесом) structures, have been made by high-aspect ratio micromolding.

- (Интеграция с Si-ИС) Capitalizing on the low deposition temperatures, an integrated MEMS fabrication process with Si ICs has been demonstrated.

- In this process, CMOS structures are first fabricated on Si wafers.

- Poly-SiGe mechanical structures are then surface micromachined using a poly-Ge sacrificial layer.

(Вертикальное расположение Si/SiGe/Poly-Ge technology)

- A significant advantage of this design is that the MEMS structure is positioned directly above the CMOS structure, thus reducing the parasitic capacitance and contact resistance characteristic of interconnects associated with side-by-side integration schemes.

- Use of $H_2O_2$ as the sacrificial etchant means that no special protective layers are required to protect the underlying CMOS layer during release.

- In addition to its utility as a material for integrated MEMS devices, poly-SiGe has been identified as a material well suited for micromachined thermopiles (термоэлементы) due to its lower thermal conductivity relative to Si.

# Metals

- Metallic thin films are used in many different capacities ranging from etch masks used in device fabrication to interconnects and structural elements in microsensors and microactuators.

- Metallic thin films can be deposited using a wide range of techniques, including evaporation, sputtering, CVD, and electroplating.

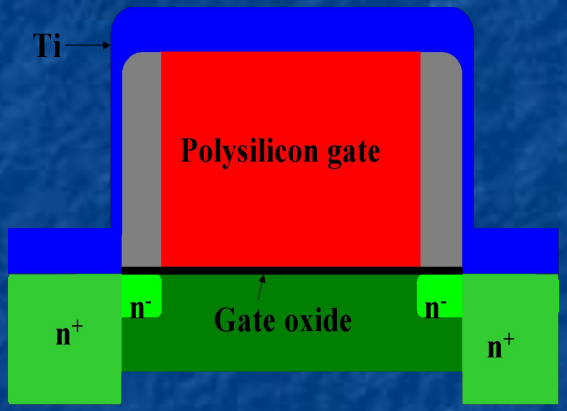
Table 2.3 List of Selected Metals That Can Be Deposited As Thin Films (Up to a Few μm in Thickness) with Corresponding Electrical Resistivities and Typical Areas of Application

| *Metal* | *ρ (μΩ-cm)* | *Typical Areas of Application* |
|---|---|---|
| Ag | 1.58 | Electrochemistry |
| Al | 2.7 | Electrical interconnects; optical reflection in the visible and the infrared |
| Au | 2.4 | High-temperature electrical interconnects; optical reflection in the infrared; electrochemistry; corrosion-resistant contact; wetting layer for soldering |
| Cr | 12.9 | Intermediate adhesion layer |
| Cu | 1.7 | Low-resistivity electrical interconnects |
| Indium-tin oxide (ITO) | 300–3,000 | Transparent conductive layer for liquid crystal displays |
| Ir | 5.1 | Electrochemistry; microelectrodes for sensing biopotentials |
| Ni | 6.8 | Magnetic transducing; solderable layer |
| NiCr | 200–500 | Thin-film laser trimmed resistor; heating element |
| Pd | 10.8 | Electrochemistry; solder-wetting layer |
| Permalloy™ ($Ni_xFe_y$) | — | Magnetic transducing |
| Pt | 10.6 | Electrochemistry; microelectrodes for sensing biopotentials; solderable layer |
| SiCr | 2,000 | Thin-film laser trimmed resistor |
| $SnO_2$ | 5,000 | Chemoresistance in gas sensors |
| TaN | 300–500 | Negative temperature coefficient of resistance (TCR) thin-film laser trimmed resistor |
| Ti | 42 | Intermediate adhesion layer |
| TiNi | 80 | Shape-memory alloy actuation |
| TiW | 75–200 | Intermediate adhesion layer; near zero TCR |
| W | 5.5 | High-temperature electrical interconnects; thermionic emitter |

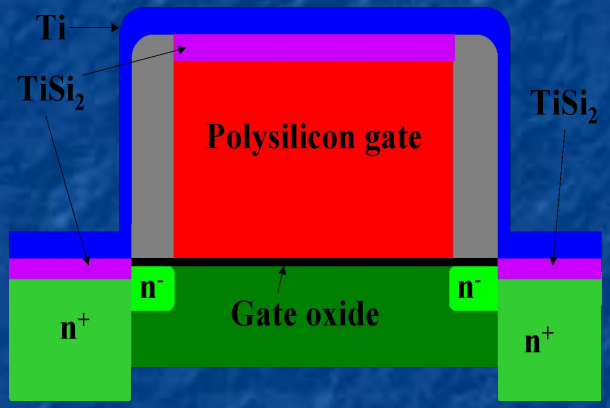
# Conducting Thin Films

- Polysilicon
- Silicides
- Aluminum alloy
- Titanium
- Titanium Nitride
- Tungsten
- Copper
- Tantalum

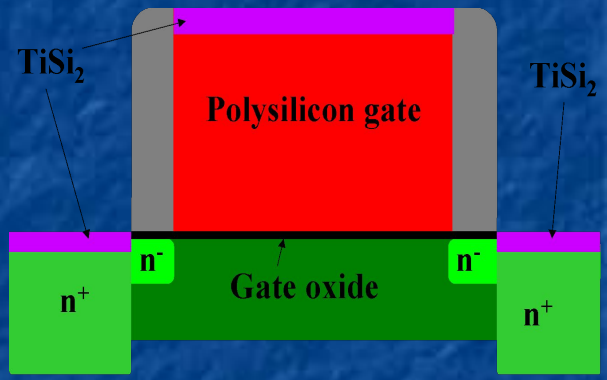
# Self-aligned Titanium Silicide Formation




Titanium deposition

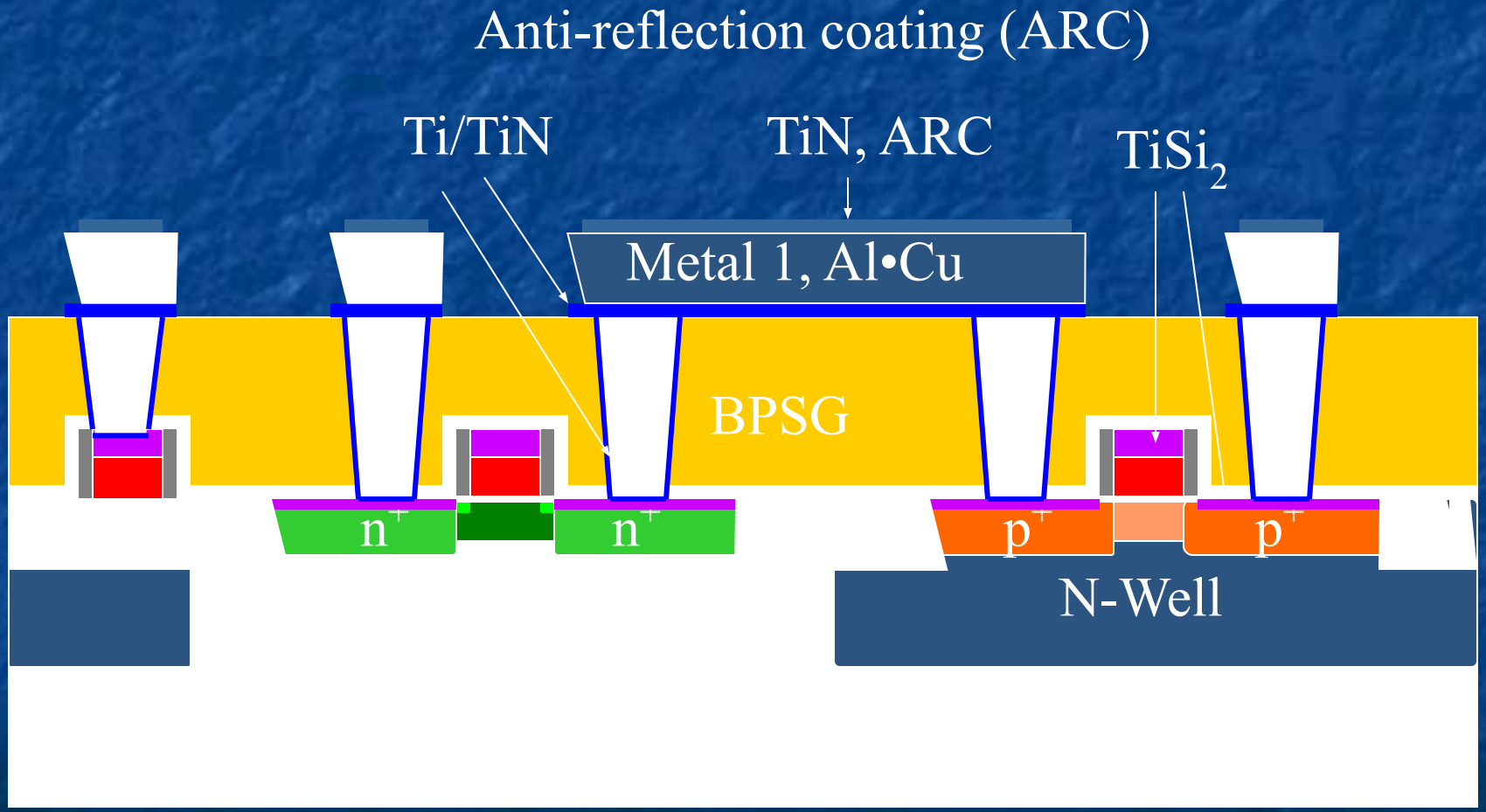



Silicide annealing




Titanium wet striping (удаление Ti)

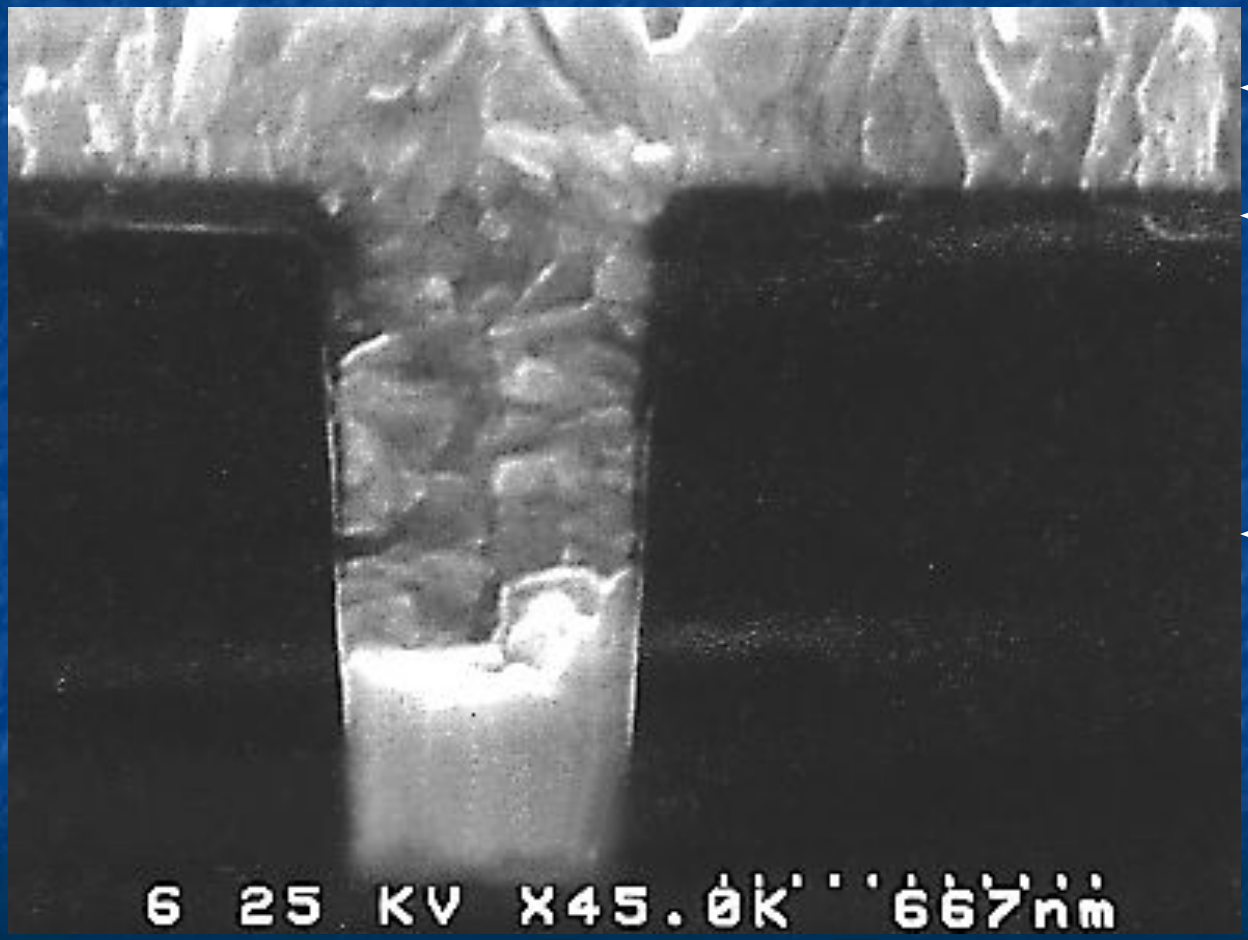
# CMOS: Standard Metallization



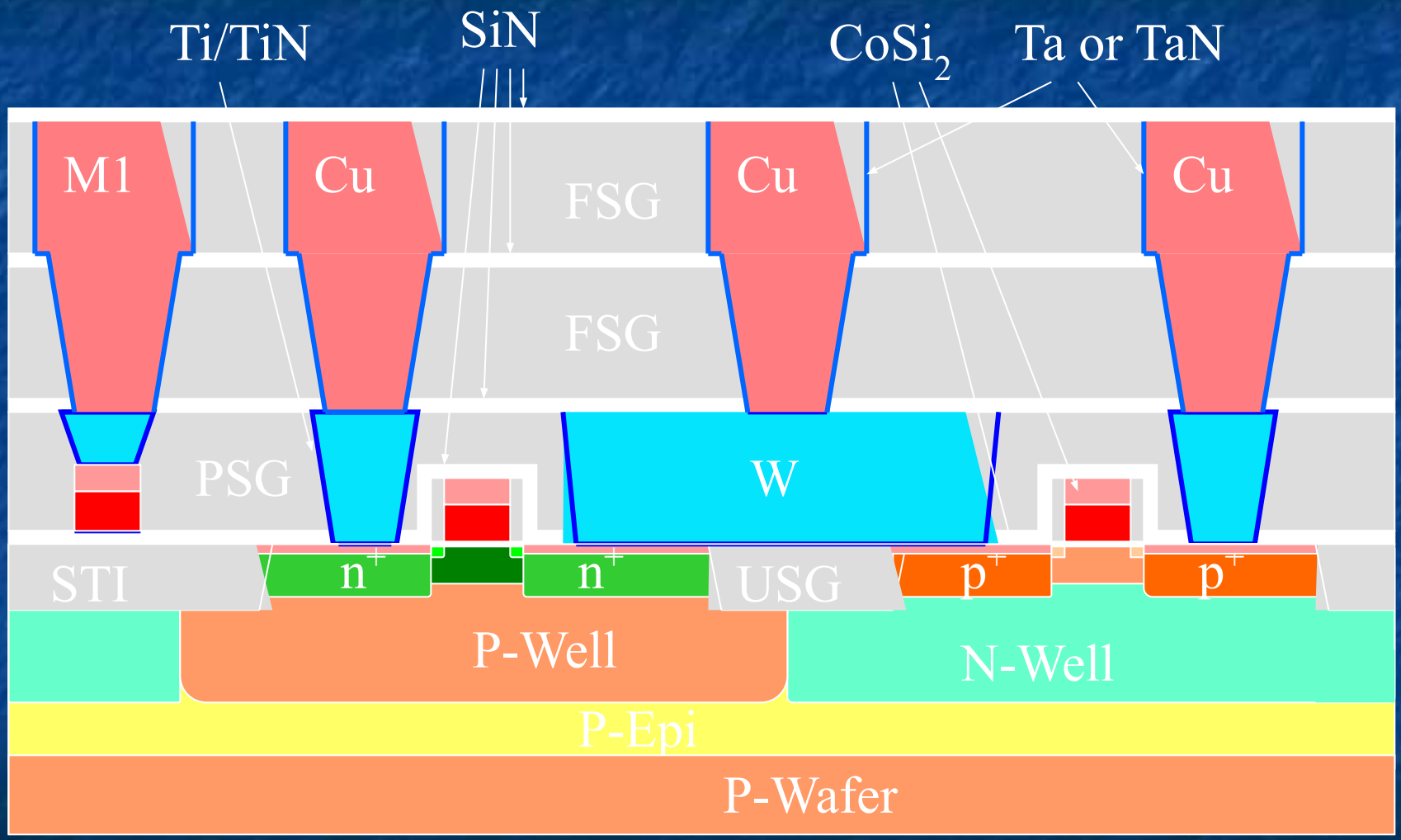
- **Fluorosilicate glass** (FSG) is a low-k dielectric (FSG) is a low-k dielectric used in between copper metal layers (FSG) is a low-k dielectric used in between copper metal layers during silicon (FSG) is a low-k dielectric used in between copper metal layers during silicon integrated circuit (FSG) is a low-k dielectric used in between copper metal layers during silicon integrated circuit fabrication (FSG) is a low-k dielectric used in between copper metal layers during silicon integrated circuit fabrication process. It has a low dielectric constant (FSG) is a low-k dielectric used in between copper metal

- **Shallow trench isolation** (**STI**), also known as **Box Isolation Technique**, is an integrated circuit, is an integrated circuit feature which prevents electrical current, is an integrated circuit feature which prevents electrical current leakage, is an integrated circuit feature which prevents electrical current leakage between adjacent semiconductor device, is an integrated circuit feature which prevents electrical current leakage between adjacent semiconductor device components. STI is generally used on CMOS, is an integrated circuit feature which prevents electrical current leakage between adjacent semiconductor device components. STI

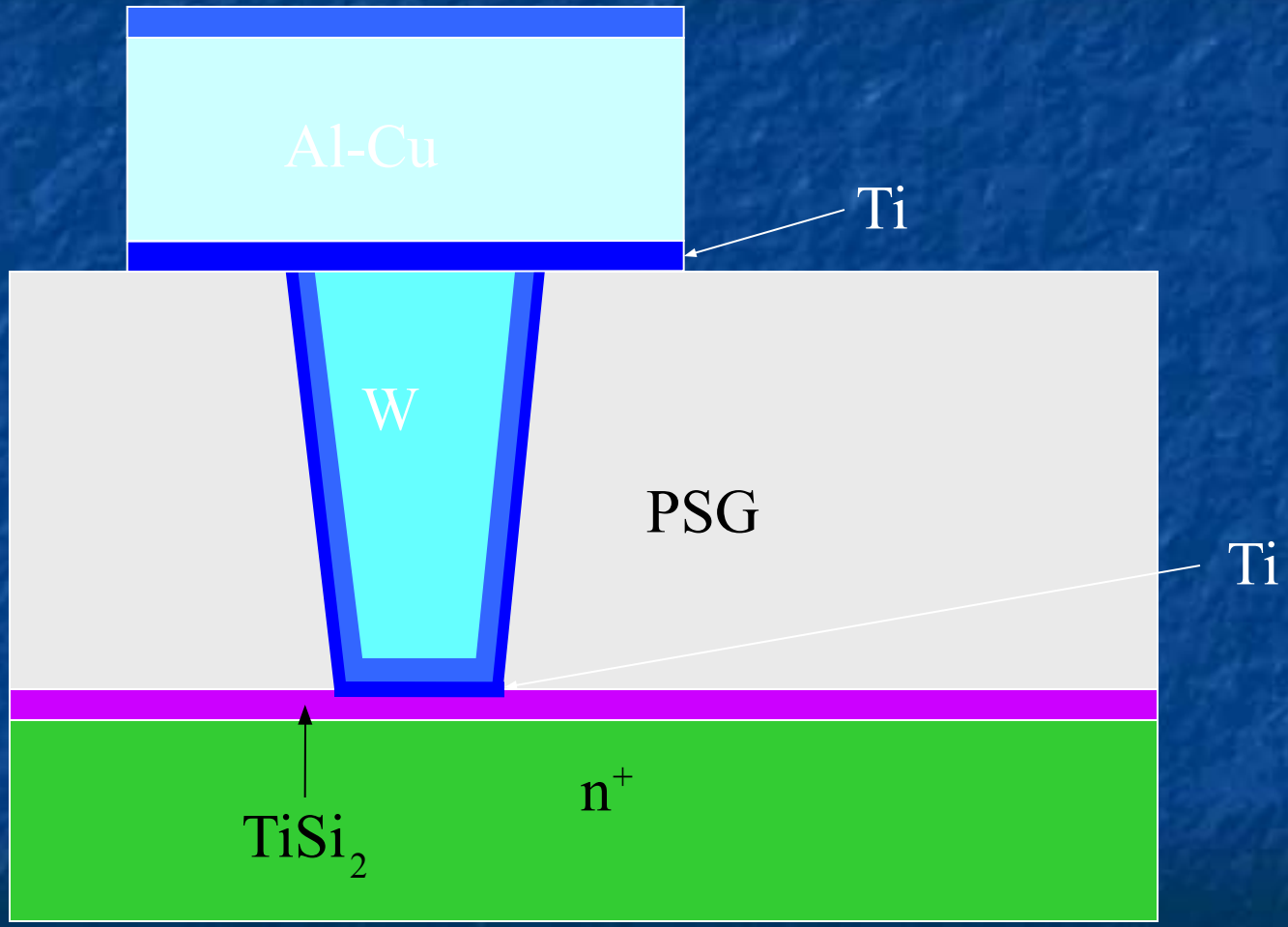
# W Plug and TiN/Ti Barrier/Adhesion Layer



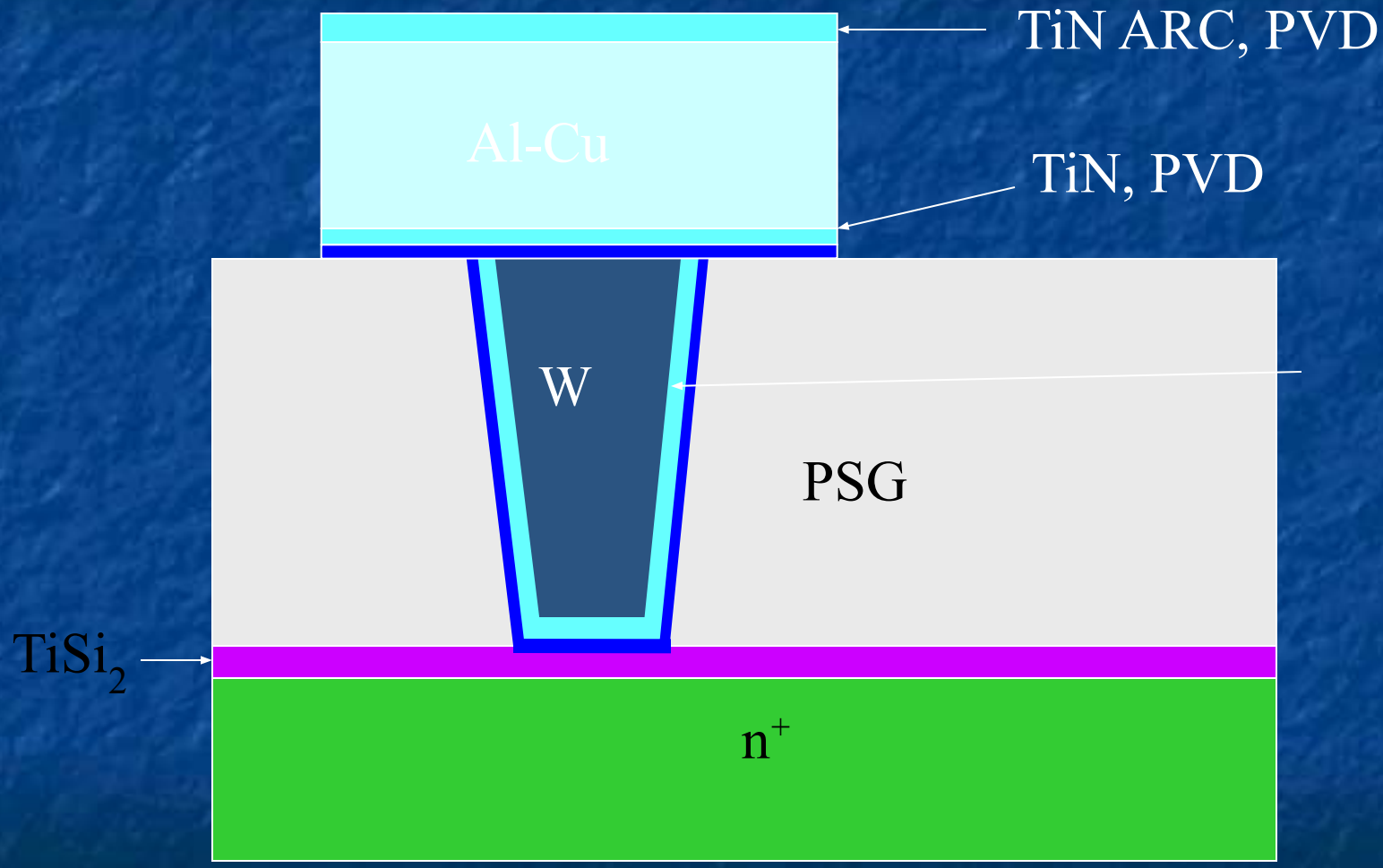
# Copper Metallization



# Applications of Titanium



# Three Applications of TiN



- Aluminum (Al) and gold (Au) are among the most widely employed metals in microfabricated electronic and MEM devices, as a result of their useas innerconnect and packaging materials.
- In addition to these critical electrical functions, Al and Au are also desirable as electromechanical materials.

- One such example is the use of Au micromechanical switches for RF MEMS.

- For conventional RF applications, chip level switching is currently performed using FET (полевой транзистор)- and PIN diode-based solid state devices fabricated from gallium arsenide (GaAs) substrates.

http://airccse.com/eeij/papers/1114eeij03.pdf

- Electrical Engineering: An International Journal (EEIJ), Vol. 1, No. 1, June 2014

A NOVEL SEESAW-TYPE RF MEMS SWITCH WITH MINIMUM STRESS IN MEMBRANE FOR RF FRONTEND APPLICATIONS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- ABSTRACT
- In this paper a novel RF MEMS switch design with a seesaw-type movable part to implement a metallic connection across a broken CPW transmission **(Coplanar waveguide)** line has been proposed and tested. The switching action is done through two separate pull-up electrodes. For this design with a 5-10 µm gap between the suspended membrane and the pull-down electrodes, applying an actuation voltage of 5-10V, dynamic analysis shows a switching time of less than 10 µs. Unlike in other MEMS switches designed earlier for RF devices the proposed work in this report works with two supply lines switched seamlessly. The bending of the membrane is considerably reduced in this type of switch as the actuation electrodes are in the outer end and the signal lines between the pivot arrangement and electrode. The existing switches implement a single signal line and it is switched on and off but in the proposed switch two supply lines on both sides of the substrate are kept and are switched from one to the other by the see-saw operation of the membrane.

- Unfortunately, these devices suffer (страдают) from insertion losses and poor electrical solation.

- In an effort to develop replacements for GaAs-based solid state switches, *Hyman* et al. reported the development of an electrostatically actuated, cantilever-based micromechanical switch fabricated on GaAs substrates.

- The trilayer cantilever structure was chosen to minimize the deleterious effects of thermal and process-related stress gradients in order to produce unbent (не разогнутые балки) and thermally stable beams.
- After deposition and pattering, the cantilevers were released in HF.

- The processing steps proved to be completely compatible with GaAs substrates.
- The released cantilevers demonstrated switching speeds better than 50μs at 25V with contact lifetimes exceeding $10^9$ cycles.

- In a second example from RF MEMS, *Chang* et al. reported the fabrication of an Al-based micromachined switch as an alternative to GaAs FETs and PIN diodes.

- In contrast to the work by *Hyman* et al., this switch utilizes the differences in the residual stresses in Al and Cr thin films to create bent (изгибать) cantilever switches that capitalize on the stress differences in the materials.

- Each switch is comprised of a series of linked bimorph cantilevers designed in such a way that the resulting structure bends significantly out of the plane of the wafer due to the stress differences in the bimorph.
- The switch is drawn closed by electrostatic attraction.
- The bimorph consists of metals that can easily be processed with GaAs wafers, thus making integration with GaAs devices possible.

- The released switches were relatively slow, at 10ms, but an actuation voltage of only 26V was needed to close the switch.
- Thin-film metallic alloys that exhibit the shapememory effect are of particular interest to the MEMS community for their potential in microactuators.
- The shape-memory effect relies on the reversible transformation from a ductile (эластичный) martensite phase to a stiff (жесткий) austenite phase in the material with the application of heat.

- The reversible phase change allows the shape-memory effect to be used as an actuation mechanism, since the material changes shape during the transition.

- It has been found that high forces and strains can be generated from shape-memory thin films at reasonable power inputs, thus enabling shape-memory actuation to be used in MEMS-based microfluidic devices, such as microvalves and micropumps.

- Titanium-nickel (TiNi) is among the most popular of the shape-memory alloys, owing to its high actuation work density (50MJ/m3) and large bandwidth (up to 0.1kHz).

- TiNi is also attractive because conventional sputtering techniques can be employed to deposit thin films, as detailed in a recent report by *Shih* et al.

- In this study, TiNi films were deposited by co-sputtering elemental Ti and Ni targets, and a co-sputtering TiNi alloy and elemental Ti targets.

- It was reported that co-sputtering from TiNi and Ti targets produced better films due to process variations related to the roughening of the Ni target in the case of Ti and Ni co-sputtering. The TiNi/Ti co-sputtering process has been used to produce shape-memory material for a silicon spring-based microvalve.

- Use of thin-film metal alloys in magnetic actuator systems is another example of the versatility of metallic materials in MEMS.
- Magnetic actuation in microdevices generally requires the magnetic layers to be relatively thick (tens to hundreds of microns) to generate magnetic fields of sufficient strength to generate the desired actuation.
- To this end, magnetic materials are often deposited by thick film methods, such as electroplating.