INTEL 8051
INSTRUCTION DEFINITIONS

ACALL addr11

Function: Absolute Call

Description: ACALL unconditionally calls a subroutine located at the indicated address. The instruction increments the PC twice to obtain the address of the following instruction, then pushes the 16-bit result onto the stack (low-order byte first) and increments the Stack Pointer twice. The destination address is obtained by successively concatenating the five high-order bits of the incremented PC, opcode bits 7-5, and the second byte of the instruction. The subroutine called must therefore start within the same 2K block of the program memory as the fIrst byte of the instruction following ACALL. No flags are affected.

Example: Initially SP equals 07H. The label "SUBRTN" is at program memory location 0345 H. After executing the instruction,

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ACALL SUBRTN

at location 0123H, SP will contain 09H, internal RAM locations 08H and 09H will contain

25H and 01H, respectively, and the PC will contain 0345H.

Bytes: 2

Cycles: 2

Encoding:

a10 a9 a8 1	0 0 0 1	a7 a6 a5 a4	a3 a2 a1 a0

Operation: ACALL
(PC) ← (PC) + 2
(SP) ← (SP) + 1
«SP» ← (PC7-0)
(SP) ←(SP) + 1
«SP» ←(PC15-8)
(PC10-0) ← page address

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ADD A, <src-byte >

Function: Add

Description: ADD adds the byte variable indicated to the Accumulator, leaving the result in the Accumulator. The carry and auxiliary-carry flags are set, respectively, if there is a carry-out from bit 7 or bit 3, and cleared otherwise. When adding unsigned integers, the carry flag indicates an overflow occurred.

OV is set if there is a carry-out of bit 6 but not out of bit 7, or a carry-out of bit 7 but not bit 6; otherwise OV is cleared. When adding signed integers, OV indicates a negative number produced as the sum of two positive operands, or a positive sum from two negative operands.

Four source operand addressing modes are allowed: register, direct, register-indirect, or immediate.

Example: The Accumulator holds OC3H (11000011B) and register 0 holds OAAH (101010l0B). The instruction,

```
ADD A,R0
```

will leave 6DH (01101101B) in the Accumulator with the AC flag cleared and both the carry flag and OV set to 1.

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ADD A,Rn

Bytes: 1

Cycles: 1

Encoding:

0 0 1 0	1 r r r

Operation: ADD

(A) ← (A) + (Rn)

ADD A,direct

Bytes: 2

Cycles: 1

Encoding:

0 0 1 0	0 1 0 1	direct address

Operation: ADD

(A) ← (A) + (direct)

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ADDC A, < src-byte >

Function: Add with Carry

Description: ADDC simultaneously adds the byte variable indicated, the carry flag and the Accumulator contents, leaving the result in the Accumulator. The carry and auxiliary-carry flags are set, respectively, if there is a carry-out from bit 7 or bit 3, and cleared otherwise. When adding unsigned integers, the carry flag indicates an overflow occurred.

OV is set if there is a carry-out of bit 6 but not out of bit 7, or a carry-out of bit 7 but not out of bit 6; otherwise OV is cleared. When adding signed integers, OV indicates a negative number produced as the sum of two positive operands or a positive sum from two negative operands.

Four source operand addressing modes are allowed: register, direct, register-indirect, or immediate.

Example: The Accumulator holds OC3H (1 100001 1B) and register 0 holds OAAH (10101010B) with the carry flag set. The instruction,

```
ADDC A,R0
```

wi11 leave 6EH (011011l0B) in the Accumulator with AC cleared and both the Carry flag and OV set to 1.

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ADDC A,Rn

Bytes: 1

Cycles: 1

Encoding

0 0 1 1	1 r r r

Operation: ADDC

(A)← (A) + (C) + (Rn)

ADDC A,direct

Bytes: 2

Cycles: 1

Encoding:

0 0 1 1	0 1 0 1	direct address

Operation: ADDC

(A)← (A) + (C) + (direct)

INSTRUCTION DEFINITIONS

ADDC A,@Ri

Bytes: 1

Cycles: 1

Encoding:

0 0 1 1	0 1 1 i

Operation: ADDC

(A) ← (A) + (C) +(RJ)

ADDC A, # data

Bytes: 2

Cycles: 1

Encoding:

0 0 1 1	0 1 0 0	immediate data

Operation: ADDC

(A) ← (A) + (C) + #data

INSTRUCTION DEFINITIONS

<u>AJMP addr11</u>

Function: Absolute Jump

Description: AJMP transfers program execution to the indicated address, which is formed at run-time by concatenating the high-order five bits of the PC (*after* incrementing the PC twice), opcode bits 7-5, and the second byte of the instruction. The destination must therefore be within the same 2K block of program memory as the first byte of the instruction following AJMP.

Example: The label "JMPADR" is at program memory location 0123H. The instruction,

AJMP JMPADR

is at location 0345H and will load the PC with 0123H.

Bytes: 2

Cycles: 2

Encoding:

a10 a9 a8 0	0 0 0 1	a7 a6 a5 a4	a3 a2 a1 a0

Operation: AJMP

(PC) $\leftarrow$ (PC) + 2

(PC10-0) $\leftarrow$ page address

INSTRUCTION DEFINITIONS

ANL < dest-byte > , < src-byte >

Function: Logical-AND for byte variables

Description: ANL performs the bitwise logical-AND operation between the variables indicated and stores the results in the destination variable. No flags are affected.

The two operands allow six addressing mode combinations. When the destination is the Accumulator, the source can use register, direct, register-indirect, or immediate addressing; when the destination is a direct address, the source can be the Accumulator or immediate data.

Note: When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, *not* the input pins.

Example: If the Accumulator holds OC3H (ll0000llB) and register 0 holds 55H (01010101B) then the instruction,

ANL A,R0

will leave 4lH (01000001B) in the Accumulator.

When the destination is a directly addressed byte, this instruction will clear combinations of bits in any RAM location or hardware register. The mask byte detonating the pattern of bits to be cleared would either be a constant contained in the instruction or a value computed in the Accumulator at run-time. The instruction,

INSTRUCTION DEFINITIONS

ANL P1, #01110011B

will clear bits 7, 3, and 2 of output port 1.

<u>**ANL** A,Rn</u>

Bytes: 1

Cycles: 1

Encoding:

0 1 0 1	1 r r r

Operation: ANL

$(A) \leftarrow (A)\ 1 \wedge (Rn)$

<u>**ANL A,direct**</u>

Bytes: 2

Cycles:1

Encoding:

0 1 0 1	0 1 0 1	direct address

Operation: ANL

$(A) \leftarrow (A) \wedge (direct)$

INSTRUCTION DEFINITIONS

<u>ANL A,@Ri</u>

Bytes: 1

Cycles: 1

Encoding:

0 1 0 1	0 1 1 i

Operation: ANL

(A) ← (A) ∧((Ri))

<u>ANL A, # data</u>

Bytes: 2

Cycles: 1

Encoding:

0 1 0 1	0 1 0 0		immediate data

Operation: ANL

(A) ← (A) ∧#data

INSTRUCTION DEFINITIONS

ANL direct,A

Bytes: 2

Cycles: 1

Encoding:

0 1 0 1	0 0 1 0	direct address

Operation: ANL

(direct) ← (direct) ∧ (A)

ANL direct, # data

Bytes: 3

Cycles: 2

Encoding:

0 1 0 1	0 0 1 1	direct address	immediate data

Operation: ANL

(direct) ← (direct) ∧#data

INSTRUCTION DEFINITIONS

ANL C, <src-bit>

Function: Logical-AND for bit variables

Description: If the Boolean value of the source bit is a logical 0 then clear the carry flag; otherwise leave the carry flag in its current state. A slash ("I") preceding the operand in the assembly language indicates that the logical complement of the addressed bit is used as the source value, but the source bit itself is not affected. No other flags are affected.

Only direct addressing is allowed for the source operand.

Example: Set the carry flag if, and only if, P1.0 = 1, ACe. 7 = 1, and OV = 0:

```
MOV C,P1.0 ;LOAD CARRY WITH INPUT PIN STATE
ANL C,ACC.7 ;AND CARRY WITH ACCUM. BIT 7
ANL C,/OV ;AND WITH INVERSE OF OVERFLOW FLAG
```

ANL C,bit

Bytes: 2

Cycles: 2

Encoding:

Operation: ANL

$(C) \leftarrow (C)\ 1 \wedge\ (bit)$

INSTRUCTION DEFINITIONS

<u>CJNE < dest-byte > , < src-byte >, rei</u>

Function: Compare and Jump if Not Equal.

Description: CJNE compares the magnitudes of the first two operands, and branches if their values are not equal. The branch destination is computed by adding the signed relative-displacement in the last instruction byte to the PC, after incrementing the PC to the start of the next instruction. The carry flag is set if the unsigned integer value of <dest-byte> is less than the unsigned integer value of < src-byte > ; otherwise, the carry is cleared. Neither operand is affected.

The first two operands allow four addressing mode combinations: the Accumulator may be compared with any directly addressed byte or immediate data, and any indirect RAM location or working register can be compared with an immediate constant.

Example: The Accumulator contains 34H. Register 7 contains 56H. The first instruction in the sequence,

```
                CJNE R7,#60H, NOT_EQ
;     …   …..             ; R7 = 60H.
NOT_EQ:     JC   REQ_LOW   ; IFR7 < 60H
;     …   …..             ; R7> 6OH.
```

sets the carry flag and branches to the instruction at label NOTJQ. By testing the carry flag, this instruction determines whether R 7 is greater or less than 60H.

If the data being presented to Port I is also 34H, then the instruction,

WAIT: CJNE A,PI,WAIT

clears the carry flag and continues with the next instruction in sequence, since the Accumulator does equal the data read from PI. (If some other value was being input on PI, the program will loop at this point until the PI data changes to 34H.)

CJNE A,direct,rel

Bytes: 3

Cycles:

Encoding:

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Operation: (PC) ← (PC) + 3

IF (A) < > (direct)

THEN

(PC) +- (PC) + *relative offtet*

IF (A) < *(direct)*

THEN

(C) ← 1

ELSE

(C) ← 0

CLR bit

Function: Clear bit

Description: The indicated bit is cleared (reset to zero). No other flags are affected. CLR can operate on the carry flag or any directly addressable bit.

Example: Port 1 has previously been written with 5DH (01011101B). The instruction,

CLR P1.2

will leave the port set to 59H (01011001B).

INSTRUCTION DEFINITIONS

CPL bit

Function: Complement bit

Description: The bit variable specified is complemented. A bit which had been a one is changed to zero and vice-versa. No other flags are affected. CLR can operate on the carry or any directly addressable bit.

Note: When this instruction is used to modify an output pin, the value used as the original data will be read from the output data latch, *not* the input pin.

Example: Port 1 has previously been written with SBH (01011101B). The instruction sequence,

CPL Pl.l

CPL Pl.2

wi11 leave the port set to SBH (01011011B).

DA A

Function: Decimal-adjust Accumulator for Addition

Description: DA A adjusts the eight-bit value in the Accumulator resulting from the earlier addition of two variables (each in packed-BCD format), producing two four-bit digits. Any ADD or ADDC instruction may have been used to perform the addition.

If Accumulator bits 3-0 are greater than nine (xxxx1010-xxxx1111), or if the AC flag is one, six is added to the Accumulator producing the proper BCD digit in the low-order nibble. This internal addition would set the carry flag if a carry-out of the low-order four-bit field propagated through all high-order bits, but it would not clear the carry flag otherwise

INSTRUCTION DEFINITIONS

If the carry flag is now set, or if the four high-order bits now exceed nine (1010xxxx-111xxxx), these high-order bits are incremented by six, producing the proper BCD digit in the high-order nibble. Again, this would set the carry flag if there was a carry-out of the high-order bits, but wouldn't clear the carry. The carry flag thus indicates if the sum of the original two BCD variables is greater than 100, allowing multiple precision decimal additions. OV is not affected.

All of this occurs during the one instruction cycle. Essentially, this instruction performs the decimal conversion by adding OOH, 06H, 6OH, or 66H to the Accumulator, depending on initial Accumulator and PSW conditions.

Note: DA A *cannot* simply convert a hexadecimal number in the Accumulator to BCD notation, nor does DA A apply to decimal subtraction.

Example: The Accumulator holds the value 56H (01010110B) representing the packed BCD digits of the decimal number 56. Register 3 contains the value 67H (01100111B) representing the packed BCD digits of the decimal number 67. The carry flag is set. The instruction sequence:

```
ADDC A,R3
DA A
```

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will first perform a standard twos-complement binary addition, resulting in the value OBEH (10111110) in the Accumulator. The carry and auxiliary carry flags will be cleared.

The Decimal Adjust instruction will then alter the Accumulator to the value 24H

(OOI00I00B), indicating the packed BCD digits of the decimal number 24, the low-order two digits of the decimal sum of 56,67, and the carry-in. The carry flag will be set by the Decimal Adjust instruction, indicating that a decimal overflow occurred. The true sum 56, 67, and 1 is 124.

BCD variables can be incremented or decremented by adding 01H or 99H. If the Accumulator initially holds 30H (representing the digits of 30 decimal), then the instruction sequence,

```
ADD A,#99H
DA A
```

will leave the carry set and 29H in the Accumulator, since 30 + 99 = 129. The low-order byte of the sum can be interpreted to mean 30 - 1 = 29.

Bytes: 1

Cycles: 1

Encoding:

1	1	0	1	0	1	0	0

Operation: DA

-contents of Accumulator are BCD

IF $[[(A_{3-0}) > 9] \vee [(AC) = 1]]$

THEN(A3-0) ← (A3-0) + 6

AND

IF [[(A7-4) > 9] V [(C) = 1]]

THEN (A7-4) ← (A7-4) + 6

<u>DEC byte</u>

Function: Decrement

Description: DEC byte decrements the variable indicated by 1. An original value of 00H underflows to 0FFH. No flags are affected. Four operand addressing modes are allowed: accumulator, register, direct, or register-indirect.

Note: When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, not the input pins.

Example: Register 0 contains 7FH (01111111B). Internal RAM locations 7EH and 7FH contain 00H and 40H, respectively.

The following instruction sequence,

```
DEC     @R0
DEC     R0
DEC     @R0
```

leaves register 0 set to 7EH and internal RAM locations 7EH and 7FH set to 0FFH and 3FH.

INSTRUCTION DEFINITIONS

DEC A

Bytes: 1

Cycles: 1

Encoding:

0	0	0	1	0	1	0	0

Operation: DEC

(A) ← (A) - 1

DEC Rn

Bytes: 1

Cycles: 1

Encoding:

0	0	0	1	1	r	r	r

Operation: DEC

(Rn) ← (Rn) - 1

DEC direct

Bytes: 2

Cycles: 1

Encoding:

0	0	0	1	0	1	0	1	direct address

Operation: DEC

(direct) ← (direct) – 1

DIV AB

Function: Divide

Description: DIV AB divides the unsigned eight-bit integer in the Accumulator by the unsigned eight-bit integer in register B.

The Accumulator receives the integer part of the quotient; register B receives the integer remainder. The carry and OV flags are cleared.

Exception: if B had originally contained 00H, the values returned in the Accumulator and B-register are undefined and the overflow flag are set. The carry flag is cleared in any case.

Example: The Accumulator contains 251 (0FBH or 11111011B) and B contains 18 (12H or 00010010B). The following instruction:

```
DIV    AB
```

leaves 13 in the Accumulator (0DH or 00001101B) and the value 17 (11H or 00010001B) in B, since 251 = (13 x 18) + 17. Carry and OV are both cleared.

Bytes: 1

Cycles: 4

Encoding:

Operation: DIV

$(A)_{15-8} \leftarrow (A)/(B)$

$(B)_{7-0}$

DJNZ <byte>,<rel-addr>

Function: Decrement and Jump if Not Zero

Description: DJNZ decrements the location indicated by 1, and branches to the address indicated by the second operand if the resulting value is not zero. An original value of 00H underflows to 0FFH. No flags are affected. The branch destination is computed by adding the signed relative-displacement value in the last instruction byte to the PC, after incrementing the PC to the first byte of the following instruction.

The location decremented may be a register or directly addressed byte.

Note: When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, *not* the input pins.

Example: Internal RAM locations 40H, 50H, and 60H contain the values 01H, 70H, and 15H, respectively. The following instruction sequence,

```
DJNZ 40H,LABEL_1
DJNZ 50H,LABEL_2
DJNZ 60H,LABEL_3
```

causes a jump to the instruction at label LABEL_2 with the values 00H, 6FH, and 15H in the three RAM locations. The first jump was *not* taken because the result was zero.

This instruction provides a simple way to execute a program loop a given number of times or for adding a moderate time delay (from 2 to 512 machine cycles) with a single instruction. The following instruction sequence:

```
        MOV R2, # 8
TOGGLE:     CPL P1.7
        DJNZ R2,TOGGLE
```

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toggles P1.7 eight times, causing four output pulses to appear at bit 7 of output Port 1. Each pulse lasts three machine cycles; two for DJNZ and one to alter the pin.

DJNZ Rn,rel

Bytes: 2

Cycles: 2

Encoding:

1	1	0	1	1	r	r	r	rel. address

Operation: DJNZ

(PC) ← (PC) + 2

(Rn) ← (Rn) - 1

IF (Rn) > 0 or (Rn) < 0

THEN

(PC) ← (PC) + rel

DJNZ direct,rel

Bytes: 3

Cycles: 2

Encoding:

1	1	0	1	0	1	0	1	direct address	rel. address

Operation: DJNZ

(PC) ← (PC) + 2

(direct) ← (direct) - 1

IF (direct) > 0 or (direct) < 0

THEN

(PC) ← (PC) + rel

INC <byte>

Function: Increment

Description: INC increments the indicated variable by 1. An original value of 0FFH overflows to 00H. No flags are affected. Three addressing modes are allowed: register, direct, or register-indirect.

Note: When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, not the input pins.

Example: Register 0 contains 7EH (011111110B). Internal RAM locations 7EH and 7FH contain 0FFH and 40H, respectively. The following instruction sequence:

INC @R0

INC R0

INC @R0

leaves register 0 set to 7FH and internal RAM locations 7EH and 7FH holding 00H and 41H, respectively.

INC A

Bytes: 1

Cycles: 1

Encoding:

0	0	0	0	0	1	0	0

Operation: INC

$(A) \leftarrow (A) + 1$

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INC Rn

Bytes: 1

Cycles: 1

Encoding:

0	0	0	0	1	r	r	r

Operation: INC

(Rn) ← (Rn) + 1

INC direct

Bytes: 2

Cycles: 1

Encoding:

0	0	0	0	0	1	0	1	direct address

Operation: INC

(direct)← direct) + 1

INSTRUCTION DEFINITIONS

INC DPTR

Function: Increment Data Pointer

Description: INC DPTR increments the 16-bit data pointer by 1. A 16-bit increment (modulo 2 powered to 16) is performed, and an overflow of the low-order byte of the data pointer (DPL) from 0FFH to 00H increments the high-order byte (DPH).

No flags are affected.

This is the only 16-bit register which can be incremented.

Example: Registers DPH and DPL contain 12H and 0FEH, respectively. The following instruction sequence,

INC DPTR

INC DPTR

INC DPTR

changes DPH and DPL to 13H and 01H.

Bytes: 1

Cycles: 2

Encoding:

1	0	1	0	0	0	1	1

Operation: INC

$$(DPTR) \leftarrow (DPTR) + 1$$

INSTRUCTION DEFINITIONS

JB blt,rel

Function: Jump if Bit set

Description: If the indicated bit is a one, JB jump to the address indicated; otherwise, it proceeds with the next instruction. The branch destination is computed by adding the signed relative-displacement in the third instruction byte to the PC, after incrementing the PC to the first byte of the next instruction. The bit tested is not modified. No flags are affected.

Example: The data present at input port 1 is 11001010B. The Accumulator holds 56 (01010110B). The following instruction sequence,

```
JB   P1.2,LABEL1
JB   ACC. 2,LABEL2
```

causes program execution to branch to the instruction at label LABEL2.

Bytes: 3

Cycles: 2

Encoding:

0	0	1	0	0	0	0	0	bit address	rel. address

Operation: JB

$(PC) \leftarrow (PC) + 3$

IF $(bit) = 1$

THEN

$(PC) \leftarrow (PC) + rel$

JBC bit,rel

Function: Jump if Bit is set and Clear bit

Description: If the indicated bit is one, JBC branches to the address indicated; otherwise, it proceeds with the next instruction. *The bit will not be cleared if it is already a zero*. The branch destination is computed by adding the signed relative-displacement in the third instruction byte to the PC, after incrementing the PC to the first byte of the next instruction. No flags are affected.

Note: When this instruction is used to test an output pin, the value used as the original data will be read from the output data latch, *not* the input pin.

Example: The Accumulator holds 56H (01010110B). The following instruction sequence,

JBC ACC.3,LABEL1

JBC ACC.2,LABEL2

causes program execution to continue at the instruction identified by the label LABEL2, with the Accumulator modified to 52H (01010010B).

Bytes: 3

Cycles: 2

Encoding:

0	0	0	1	0	0	0	0	bit address	rel. address

Operation: JBC

(PC) ← (PC) + 3

IF (bit) = 1

THEN

(bit) ← 0

(PC) ← (PC) +rel

JC rel

Function: Jump if Carry is set

Description: If the carry flag is set, JC branches to the address indicated; otherwise, it proceeds with the next instruction. The branch destination is computed by adding the signed relative-displacement in the second instruction byte to the PC, after incrementing the PC twice. No flags are affected.

Example: The carry flag is cleared. The following instruction sequence,

```
JC LABEL1
CPL C
JC LABEL 2
```

sets the carry and causes program execution to continue at the instruction identified by the label LABEL2.

Bytes: 2

Cycles: 2

Encoding:

0	1	0	0	0	0	0	0		rel. address

Operation: JC

$(PC) \leftarrow (PC) + 2$

IF $(C) = 1$

THEN

$(PC) \leftarrow (PC) + rel$

INSTRUCTION DEFINITIONS

JMP @A+DPTR

Function: Jump indirect

Description: Add the eight-bit unsigned contents of the Accumulator with the sixteen-bit data pointer, and load the resulting sum to the program counter. This will be the address for subsequent instruction fetches. Sixteen-bit addition is performed (modulo 216): a carry-out from the low-order eight bits propagates through the higher-order bits. Neither the Accumulator nor the Data Pointer is altered. No flags are affected.

Example: An even number from 0 to 6 is in the Accumulator. The following sequence of instructions will branch to one of four AJMP instructions in a jump table starting at JMP _TBL:

```
         MOV       DPTR, #JMP _TBL
         JMP  @A+DPTR
JMP_TBL:     AJMP     LABELO
         AJMP      LABEL1
         AJMP     LABEL2
         AJMP     LABEL3
```

If the Accumulator equals 04H when starting this sequence, execution will jump to label LABEL2. Remember that AJMP is a two-byte instruction, so the jump instructions start at every other address.

INSTRUCTION DEFINITIONS

Bytes: 1

Cycles: 2

Encoding:

0 1 1 1	0 0 1 1

Operation: JMP

(PC) ~ (A) + (DPTR)

JNB bit,rel

Function: Jump if Bit Not set

Description: If the indicated bit is a zero, branch to the indicated address; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the third instruction byte to the PC, after incrementing the PC to the first byte of the next instruction. The bit tested is not modified. No flags are affected.

Example: The data present at input port 1 is 1 10010 l0B. The Accumulator holds 56H (010101 l0B). The instruction sequence,

JNB P1.3,LABELl

JNB ACC.3,LABEL2

will cause program execution to continue at the instruction at label LABEL2.

Bytes: 1

Cycles: 2

Encoding:

0 0 1 1	0 0 0 0	bit address	rel. address

INSTRUCTION DEFINITIONS

Operation JNB

(PC) ← (PC) + 3

IF (bit) = 0

THEN (PC) ← (PC) + reI.

<u>JZ rei</u>

Function: Jump if Accumulator Zero

Description: If all bits of the Accumulator are zero, branch to the address indicated; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the second instruction byte to the PC, after incrementing the PC twice. The Accumulator is not modified. No flags are affected.

Example: The Accumulator originally contains OIH. The instruction sequence,

JZ LABEL1

DEC A

JZ LABEL2

will change the Accumulator to OOH and cause program execution to continue at the instruction identified by the label LABEL2.

INSTRUCTION DEFINITIONS

Bytes: 2

Cycles: 2

Encoding:

0 0 0 1	0 0 1 0	addr15-addr8	addr7-addr0

Operation: LCALL

(PC) ← (PC) + 3

(SP) ←(SP) + 1

«SP» ←(PC7-O)

(SP) ←(SP) + 1

«SP» ←(PC15-S)

(PC) ← addr15-O

<u>LJMP addr16</u>

Function: Long Jump

Description: LJMP causes an unconditional branch to the indicated address, by loading the high-order and low-order bytes of the PC (respectively) with the second and third instruction bytes. The destination may therefore be anywhere in the full 64K program memory address space. No flags are affected.

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Example: The label "JMPADR" is assigned to the instruction at program memory location 1234H. The instruction,

LJMP JMPADR

at location 0123H will load the program counter with 1234H.

Bytes: 3

Cycles: 2

Encoding:

0 0 0 0	0 0 1 0	addr15-addr8	addr7-addr0

Operation: LJMP

(PC) ← addf15-O

<u>MOV < dest-byte > ,<src-byte></u>

Function: Move byte variable

Description: The byte variable indicated by the second operand is copied into the location specified by the first operand. The source byte is not affected. No other register or flag is affected.

This is by far the most flexible operation. Fifteen combinations of source and destination addressing modes are allowed.

Example: Internal RAM location 30H holds 40H. The value of RAM location 40H is 10H. The data present at input port 1 is 11001010B (OCAH).

INSTRUCTION DEFINITIONS

```
MOV RO,#30H   ;RO <= 30H
MOV A,@RO     ;A <= 40H
MOV Rl,A              ;RI <= 40H
MOV B,@RI     ;B <= lOH
MOV @RI,PI    ;RAM (40H) < = OCAH
MOV P2,PI     ;P2 #OCAH
```

leaves the value 30H in register 0, 40H in both the Accumulator and register I, l0H in register B, and OCAH (1 100 10 l0B) both in RAM location 40H and output on port 2

MOV A,Rn

Bytes: 1

Cycles: 1

Encoding:

1 1 1 0	1 r r r

Operation: MOV

$(A) \leftarrow (Rn)$

INSTRUCTION DEFINITIONS

MOV A,direct

Bytes: 2

Cycles:

Encoding:

1 1 1 0	0 1 0 1	direct address

Operation: MOV

(A) ←(direct)

MOV A,ACC is not a valid instruction.

MOV A,@Ri

Bytes: 1

Cycles: 1

Encoding:

1 1 1 0	0 1 1 i

Operation: MOV

(A) ←(Ri)

INSTRUCTION DEFINITIONS

MOV A, # data

Bytes: 2

Cycles: 1

Encoding:

0 1 1 1	0 1 0 0	immediate data

Operation: MOV

(A) ← #data

MOV Rn,A

Bytes: 1

Cycles: 1

Encoding:

1 1 1 1	1 r r r

Operation: MOV

(Rn) ← (A)

INSTRUCTION DEFINITIONS

MOV Rn,direct

Bytes: 2

Cycles: 2

Encoding:

1 0 1 0	1 r r r		direct addr.

Operation: MOV

(Rn) ← (direct)

MOV Rn, # data

Bytes: 2

Cycles: 2

Encoding:

0 1 1 1	1 r r r		immediate data

Operation: MOV

(Rn) ← #data

INSTRUCTION DEFINITIONS

MOV direct,A

Bytes: 2

Cycles: 1

Encoding:

Operation: MOV

(direct) ← (A)

MOV direct,Rn

Bytes: 2

Cycles: 2

Encoding:

Operation: MOV

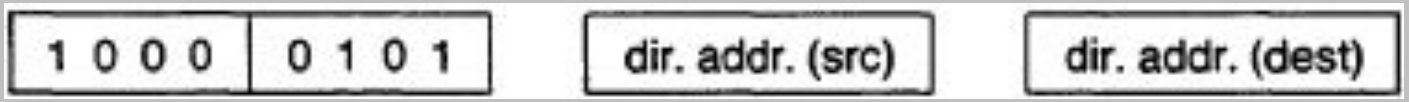
(direct) ← (Rn)

MOV direct,direct

Bytes: 3

Cycles: 2

Encoding:



INSTRUCTION DEFINITIONS

Operation: MOV

(direct) ← (direct)

MOV direct,@Ri

Bytes: 2

Cycles: 2

Encoding:

1 0 0 0	0 1 1 i	direct addr.

Operation: MOV

(direct) ← ((Ri))

MOV direct, # data

Bytes: 3

Cycles: 2

Encoding:

0 1 1 1	0 1 0 1	direct address	immediate data

Operation: MOV

(direct) ← #data

INSTRUCTION DEFINITIONS

MOV @Ri,A

Bytes: 1

Cycles: 1

Encoding:

1 1 1 1	0 1 1 i

Operation: MOV

((Ri)) ← (A)

MOV @Ri,direct

Bytes: 2

Cycles: 2

Encoding:

1 0 1 0	0 1 1 i	direct addr.

Operation: MOV

((Ri)) ← (direct)

INSTRUCTION DEFINITIONS

MOV @Ri,#data

Bytes: 2

Cycles: 1

Encoding:

Operation: MOV

$((RI)) \leftarrow \#data$

<u>MOV < dest-bit > , < src-bit ></u>

Function: Move bit data

Description: The Boolean variable indicated by the second operand is copied into the location specified by the first operand. One of the operands must be the carry flag; the other may be any directly addressable bit. No other register or flag is affected.

Example: The carry flag is originally set. The data present at input Port 3 is 1 1 00010 1B. The data previously written to output Port 1 is 35H (00110101B).

```
MOV P1.3,C
MOV C,P3.3
MOV P1.2,C
```

will leave the carry cleared and change Port 1 to 39H (0011100lB).

INSTRUCTION DEFINITIONS

MOV C,bit

Bytes: 2

Cycles: 1

Encoding:

1 0 1 0	0 0 1 0	bit address

Operation: MOV

(C) ⟵ (bit)

MOV bit,C

Bytes: 2

Cycles: 2

Encoding:

1 0 0 1	0 0 1 0	bit address

Operation: MOV

(bit) ⟵ (C)

MOV DPTR,#data16

Function: Load Data Pointer with a 16-bit constant

Description: The Data Pointer is loaded with the 16-bit constant indicated. The 16-bit constant is loaded into the second and third bytes of the instruction. The second byte (DPH) is the high-order byte, while the third byte (DPL) holds the low-order byte. No flags are affected.

This is the only instruction which moves 16 bits of data at once.

Example: The instruction,

MOV DPTR, # 1234H

will load the value 1234H into the Data Pointer: DPH will hold 12H and DPL will hold 34H.

Bytes: 3

Cycles: 2

Encoding:

1 0 0 1	0 0 0 0	immed. data15-8	immed. data7-0

Operation: MOV

$(DPTR) \longleftarrow \# data_{15-0}$

$DPH\ 0\ DPL \longleftarrow \# data_{15-8}\ 0\ \# data_{7-0}$

INSTRUCTION DEFINITIONS

MOVC A,@A+ <base-reg>

Function: Move Code byte

Description: The MOVC instructions load the Accumulator with a code byte, or constant from program memory. The address of the byte fetched is the sum of the original unsigned eight-bit Accumulator contents and the contents of a sixteen-bit base register, which may be either the Data Pointer or the PC. In the latter case, the PC is incremented to the address of the following instruction before being added with the Accumulator; otherwise the base register is not altered. Sixteen-bit addition is performed so a carry-out from the low-order eight bits may propagate through higher-order bits. No flags are affected.

Example: A value between 0 and 3 is in the Accumulator. The following instructions will translate the value in the Accumulator to one of four values defined by the DB (define byte) directive.

```
REL_PC: INC A
MOVC A,@A+PC
        RET
        DB   66H
        DB   77H
        DB   88H
        DB   99H
```

If the subroutine is called with the Accumulator equal to OlH, it will return with 77H in the Accumulator. The INC A before the MOVC instruction is needed to "get around" the RET instruction above the table. If several bytes of code separated the MOVC from the table, the corresponding number would be added to the Accumulator instead.

INSTRUCTION DEFINITIONS

MOVC A,@A+DPTR

Bytes: 1

Cycles: 2

Encoding:

1 0 0 1	0 0 1 1

Operation: MOVC

(A) ← ((A) + (DPT))

MOVC A,@A + PC

Bytes :1

Cycles: 2

Encoding:

1 0 0 0	0 0 1 1

Operation: MOVC

(PC) ← (PC) + 1

(A) ← ((A) + (PC))

INSTRUCTION DEFINITIONS

MOVX < dest-byte > ,<src-byte>

Function: Move External

Description: The MOVX instructions transfer data between the Accumulator and a byte of external data memory, hence the "X" appended to MOV. There are two types of instructions, differing in whether they provide an eight-bit or sixteen-bit indirect address to the external data RAM.

In the first type, the contents of RO or Rl in the current register bank provide an eight-bit address multiplexed with data on po. Eight bits are sufficient for external *1/0* expansion decoding or for a relatively small RAM array. For somewhat larger arrays, any output port pins can be used to output higher-order address bits. These pins would be controlled by an

output instruction preceding the MOVX.

In the second type of MOVX instruction, the Data Pointer generates a sixteen-bit address. P2 outputs the high-order eight address bits (the contents of DPH) while po multiplexes the low order eight bits (DPL) with data. The P2 Special Function Register retains its previous contents

while the P2 output buffers are emitting the contents of DPH. This form is faster and more efficient when accessing very large data arrays (up to 64K bytes), since no additional instructions are needed to set up the output ports.

It is possible in some situations to mix the two MOVX types. A large RAM array with its high-order address lines driven by P2 can be addressed via the Data Pointer, or with code to output high-order address bits to P2 followed by a MOVX instruction using RO or Rl.

INSTRUCTION DEFINITIONS

Example: An external 256 byte RAM using multiplexed address data lines (e.g., an Intel 8155 *RAMI I/OlTimer)* is connected to the 8051 Port O. Port 3 provides control lines for the external RAM. Ports 1 and 2 are used for nominal I/O. Registers 0 and 1 contain 12H and 34H. Location 34H of the external RAM holds the value 56H. The instruction sequence,

MOVX A,@Rl

MOVX @RO,A

copies the value 56H into both the Accumulator and external RAM location 12H.

MOVX A,@Ri

Bytes: 1

Cycles: 2

Encoding:

1 1 1 0	0 0 1 i

Operation: MOVX

(A) ⟵((Ri))

MOVX A,@DPTR

Bytes: 1

Cycles: 2

Encoding:

1 1 1 0	0 0 0 0

Operation MOVX

(A) ←((DPTR))

INSTRUCTION DEFINITIONS

<u>MOVX @Ri,A</u>

Bytes: 1

Cycles: 2

Encoding:

1 1 1 1	0 0 1 i

Operation: MOVX

((Ri)) ← (A)

<u>MOVX @DPTR,A</u>

Bytes: 1

Cycles: 2

Encoding:

1 1 1 1	0 0 0 0

Operation: MOVX

(DPTR) ← (A)

INSTRUCTION DEFINITIONS

MUL AB

Function: Multiply

Description: MUL AB multiplies the unsigned eight-bit integers in the Accumulator and register B. The low-order byte of the sixteen-bit product is left in the Accumulator, and the high-order byte in B. If the product is greater than 255 (OFFH) the overflow flag is set; otherwise it is cleared. The carry flag is always cleared.

Example: Originally the Accumulator holds the value 80 (50H). Register B holds the value 160 (OAOH). The instruction,

MUL AB

will give the product 12,800 (3200H), so B is changed to 32H (OOII00lOB) and the Accumulator is cleared. The overflow flag is set, carry is cleared.

Bytes: 1

Cycles: 4

Encoding:

1 0 1 0	0 1 0 0

Operation: MUL

$(A)_{7-0} \leftarrow (A) \times (B)$

B_{15-8}

INSTRUCTION DEFINITIONS

NOP

Function: No Operation

Description: Execution continues at the following instruction. Other than the PC, no registers or flags are affected.

Example: It is desired to produce a low-going output pulse on bit 7 of Port 2 lasting exactly 5 cycles. A simple SETB/CLR sequence would generate a one-cycle pulse, so four additional cycles must be inserted. This may be done (assuming no interrupts are enabled) with the instruction sequence,

```
CLR     P2.7
NOP
NOP
NOP
NOP
SETB    P2.7
```

Bytes: 1

Cycles: 1

Encoding:

0 0 0 0	0 0 0 0

Operation: NOP

$(PC) \leftarrow (PC) + 1$

INSTRUCTION DEFINITIONS

<u>ORL < dest-byte > < src-byte ></u>

Function: Logical-OR for byte variables

Description: ORL performs the bitwise logical-OR operation between the indicated variables, storing the results in the destination byte. No flags are affected.

The two operands allow six addressing mode combinations. When the destination is the Accumulator, the source can use register, direct, register-indirect, or immediate addressing; when the destination is a direct address, the source can be the Accumulator or immediate data.

Note: When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, *not* the input pins.

Example: If the Accumulator holds 0C3H (11000011B) and R0 holds 55H (01010101B) then the instruction,

ORL A,R0

will leave the Accumulator holding the value OD7H (11010111B).

When the destination is a directly addressed byte, the instruction can set combinations of bits in any RAM location or hardware register. The pattern of bits to be set is determined by a mask byte, which may be either a constant data value in the instruction or a variable computed in the Accumulator at run-time. The instruction,

ORL PI, #001 100 l0B

will set bits 5, 4, and 1 of output Port 1.

INSTRUCTION DEFINITIONS

ORL A,Rn

Bytes: 1

Cycles: 1

Encoding:

0 1 0 0	1 r r r

Operation: ORL

(A)← (A) V (Rn)

ORL C,<src-bit>

Function: Logical-OR for bit variables

Description: Set the carry flag if the Boolean value is a logical 1; leave the carry in its current state otherwise. A slash ("/") preceding the operand in the assembly language indicates that the logical complement of the addressed bit is used as the source value, but the source bit itself is not affected. No other flags are affected.

Example: Set the carry flag if and only if P1.0 = 1, ACC. 7 = 1, or OV = 0:

```
MOV C,P1.0 ;LOAD CARRY WITH INPUT PIN P10
ORL C,ACC.7 ;OR CARRY WITH THE ACC. BIT 7
ORL C,/OV ;OR CARRY WITH THE INVERSE OF OV.
```

<u>ORL C,bit</u>

Bytes: 2

Cycles: 2

Encoding:

0 1 1 1	0 0 1 0	bit address

Operation: ORL

(C) ←

POP direct

Function: Pop from stack.

Description: The contents of the internal RAM location addressed by the Stack Pointer is read, and the Stack Pointer is decremented by one. The value read is then transferred to the directly addressed byte indicated. No flags are affected.

Example: The Stack Pointer originally contains the value 32H, and internal RAM locations 30H through 32H contain the values 20H, 23H, and OlH, respectively. The instruction sequence,

POP DPH

POP DPL

will leave the Stack Pointer equal to the value 30H and the Data Pointer set to 0123H. At this point the instruction,

POP SP

will leave the Stack Pointer set to 20H. Note that in this special case the Stack Pointer was decremented to 2FH before being loaded with the value popped (20H).

INSTRUCTION DEFINITIONS

Bytes: 2

Cycles: 2

Encoding:

1 1 0 1	0 0 0 0		direct address

Operation: POP

(direct) ← ((SP))

(SP) ← (SP) – 1

<u>PUSH direct</u>

Function: Push onto stack

Description: The Stack Pointer is incremented by one. The contents of the indicated variable is then copied into the internal RAM location addressed by the Stack Pointer. Otherwise no flags are affected.

Example: On entering an interrupt routine the Stack Pointer contains 09H. The Data Pointer holds the value 0123H. The instruction sequence,

```
PUSH    DPL
PUSH    DPH
```

will leave the Stack Pointer set to OBH and store 23H and OlH in internal RAM locations OAH and OBH, respectively.

Bytes: 2

Cycles: 2

INSTRUCTION DEFINITIONS

Encoding:

1 1 0 0	0 0 0 0	direct address

Operation: PUSH

(SP) ← (SP) + 1

((SP)) ← (direct)

<u>RETI</u>

Function: Return from interrupt

Description: RETI pops the high- and low-order bytes of the PC successively from the stack, and restores the interrupt logic to accept additional interrupts at the same priority level as the one just processed. The Stack Pointer is left decremented by two. No other registers are affected; the PSW is *not* automatically restored to its pre-interrupt status. Program execution continues at the resulting address, which is generally the instruction immediately after the point at which the interrupt request was detected. If a lower- or same-level interrupt had been pending when the RETI instruction is executed, that one instruction will be executed before the pending interrupt is processed.

Example: The Stack Pointer originally contains the value OBH. An interrupt was detected during the instruction ending at location 0122H. Internal RAM locations OAH and OBH contain the values 23H and OlH, respectively. The instruction,

RETI

will leave the Stack Pointer equal to 09H and return program execution to location

INSTRUCTION DEFINITIONS

Bytes: 1

Cycles: 2

Encoding:

0 0 1 1	0 0 1 0

Operation: RETI

$(PC_{15\text{-}8}) \leftarrow ((SP))$

$(SP \leftarrow (SP) - 1$

$(PC_{7\text{-}0}) \leftarrow ((SP))$

$(SP) \leftarrow (SP) - 1$

INSTRUCTION DEFINITIONS

RL A

Function: Rotate Accumulator Left

Description: The eight bits in the Accumulator are rotated one bit to the left. Bit 7 is rotated into the bit 0 position. No flags are affected.

Example: The Accumulator holds the value 0CSH (11000101B). The instruction,

RL A

leaves the Accumulator holding the value 8BH (10001011B) with the carry unaffected.

Bytes: 1

Cycles: 1

Encoding:

0 0 1 0	0 0 1 1

Operation: RL

(An + 1) ← (An)   n = 0 – 6

(A0) ← (A7)

RLC A

Function: Rotate Accumulator Left through the Carry flag

Description: The eight bits in the Accumulator and the carry flag are together rotated one bit to the left. Bit 7 moves into the carry flag; the original state of the carry flag moves into the bit 0 position. No other flags are affected.

Example: The Accumulator holds the value 0CSH (11000101B), and the carry is zero. The instruction,

RLC A

leaves the Accumulator holding the value 8BH (10001010B) with the carry set.

Bytes: 1

Cycles: 1

Encoding: | 0 0 1 1 | 0 0 1 1 |

Operation: RLC

(An + 1) ← (An) n = 0 - 6

(A0) ← (C)

(C) ← (A7)

<u>RR A</u>

Function: Rotate Accumulator Right

Description: The eight bits in the Accumulator are rotated one bit to the right. Bit 0 is rotated into the bit 7 position. No flags are affected.

Example: The Accumulator holds the value 0C5H (11000101B). The instruction,

RR A

leaves the Accumulator holding the value 0E2H (11100010B) with the carry unaffected.

Bytes: 1

Cycles: 1

Encoding: | 0 0 0 0 | 0 0 1 1 |

Operation: RR

(An) ← (An + 1) n = 0 - 6

(A7) ← (A0)

INSTRUCTION DEFINITIONS

<u>RRC A</u>

Function: Rotate Accumulator Right through Carry flag

Description: The eight bits in the Accumulator and the carry flag are together rotated one bit to the right. Bit 0 moves into the carry flag; the original value of the carry flag moves into the bit 7 position. No other flags are affected.

Example: The Accumulator holds the value 0C5H (11000101B), the carry is zero. The instruction,

RRC A

leaves the Accumulator holding the value 62 (01100010B) with the carry set.

Bytes: 1

Cycles: 1

Encoding:

0 0 0 1	0 0 1 1

Operation: RRC

$(An) \leftarrow (An + 1) \quad n = 0 - 6$

$(A7) \leftarrow (C)$

$(C) \leftarrow (A0)$

INSTRUCTION DEFINITIONS

<u>SETB <bit></u>

Function: Set Bit

Description: SETB sets the indicated bit to one. SETB can operate on· the carry flag or any directly addressable bit. No other flags are affected.

Example: The carry flag is cleared. Output Port 1 has been written with the value 34H (00l10100B). The instructions,

SETB C

SETB Pl.0

will leave the carry flag set to 1 and change the data output on Port 1 to 35H (00l10101B).

<u>SETB C</u>

Bytes: 1

Cycles: 1

Encoding:

1 1 0 1	0 0 1 1

Operation:

(C) $\leftarrow$ 1

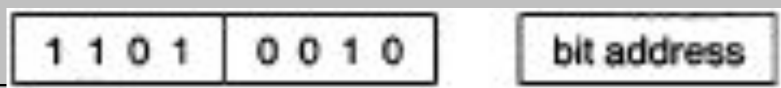
SETB bit

Bytes: 2

Cycles: 1

Encoding:

Operation:



(bit) ← 1

SJMP rel

Function: Short Jump

Description: Program control branches unconditionally to the address indicated. The branch destination is computed by adding the signed displacement in the second instruction byte to the PC, after incrementing the PC twice. Therefore, the range of destinations allowed is from 128 bytes preceding this instruction to 127 bytes following it.

Example: The label "RELADR" is assigned to an instruction at program memory location 0123H. The instruction,

SJMP RELADR

will assemble into location 0100H. After the instruction is executed, the PC will contain the value 0123H.

(*Note*: Under the above conditions the instruction following SJMP will be at l02H. Therefore, the displacement byte of the instruction will be the relative offset (0123H0102H) = 21H. Put another way, an SJMP with a displacement of 0FEH would be a one-instruction infinite loop.)

INSTRUCTION DEFINITIONS

Bytes: 2
Cycles: 2
Encoding:
Operation: SJMP

$(PC) \leftarrow (PC) + 2$

$(PC) \leftarrow (PC) + rel$

SUBB A, <src-byte>

Function: Subtract with borrow

Description: SUBB subtracts the indicated variable and the carry flag together from the Accumulator, leaving the result in the Accumulator. SUBB sets the carry (borrow) flag if a borrow is needed for bit 7, and clears C otherwise. (If C was set before executing a SUBB instruction, this indicates that a borrow was needed for the previous step in a multiple precision subtraction, so the carry is subtracted from the Accumulator along with the source operand.) AC is set if a borrow is needed for bit 3, and cleared otherwise. OV is set if a borrow is needed into bit 6, but not into bit 7, or into bit 7, but not bit 6.

When subtracting signed integers OV indicates a negative number produced when a negative value is subtracted from a positive value, or a positive result when a positive number is subtracted from a negative number.

The source operand allows four addressing modes: register, direct, register-indirect, or immediate.

INSTRUCTION DEFINITIONS

Example: The Accumulator holds 0C9H (11001001B), register 2 holds 54H (01010100B), and the carry flag is set. The instruction,

SUBB A,R2

will leave the value 74H (01110100B) in the accumulator, with the carry flag and AC cleared but OV set.

Notice that 0C9H minus 54H is 75H. The difference between this and the above result is due to the carry (borrow) flag being set before the operation. If the state of the carry is not known before starting a single or multiple-precision subtraction, it should be explicitly cleared by a CLR C instruction.

<u>SUBB A,Rn</u>

Bytes: 1

Cycles: 1

Encoding:

1 0 0 1	1 r r r

Operation: SUBB

(A) ← (A) - (C) - (Rn)

INSTRUCTION DEFINITIONS

<u>SUBB A,direct</u>

Bytes: 2

Cycles: 1

Encoding:

1 0 0 1	0 1 0 1	direct address

Operation: SUBB

(A) ← (A) - (C) - (direct)

<u>SUBB A,@Ri</u>

Bytes: 1

Cycles: 1

Encoding:

1 0 0 1	0 1 1 i

Operation: SUBB

(A) ← (A) - (C) - ((Ri))

INSTRUCTION DEFINITIONS

<u>SUBB A,#data</u>

Bytes: 2

Cycles: 1

Encoding: | 1 0 0 1 | 0 1 0 0 | | immediate data |

Operation: SUBB

(A) ← (A) - (C) - #data

<u>SWAP A</u>

Function: Swap nibbles within the Accumulator

Description: SWAP A interchanges the low- and high-order nibbles (four-bit fields) of the Accumulator (bits 3-0 and bits 7-4). The operation can also be thought of as a four-bit rotate instruction. No flags are affected.

Example: The Accumulator holds the value 0C5H (11000l0lB). The instruction,

SWAP A

leaves the Accumulator holding the value 5CH (0l011100B).

Bytes: 1

Cycles: 1

Encoding: | 1 1 0 0 | 0 1 0 0 |

Operation: SWAP

$$(A_{3-0}) \rightleftarrows (A_{7-4})$$

INSTRUCTION DEFINITIONS

<u>XCH A, < byte></u>

Function: Exchange Accumulator with byte variable

Description: XCH loads the Accumulator with the contents of the indicated variable, at the same time writing the original Accumulator contents to the indicated variable. The source/destination operand can use register, direct, or register-indirect addressing.

Example: R0 contains the address 20H. The Accumulator holds the value 3FH (00111111B). Internal RAM location 20H holds the value 7SH (01110101B). The instruction,

XCH A,@R0

will leave RAM location 20H holding the values 3FH (00111111B) and 75H (0111010lB) in the accumulator.

<u>XCH A,Rn</u>

Bytes: 1

Cycles: 1

Encoding:

1 1 0 0	1 r r r

INSTRUCTION DEFINITIONS

Operation: XCH

<u>XCH A,direct</u>

Bytes: 2

Cycles: 1

Encoding:

1 1 0 0	0 1 0 1	direct address

Operation: XCH

$$(A) \rightleftarrows (direct)$$

<u>XCH A,@Ri</u>

Bytes: 1

Cycles: 1

Encoding:

1 1 0 0	0 1 1 i

Operation: XCH

$$(A) \rightleftarrows ((Ri))$$

INSTRUCTION DEFINITIONS

XCHD A,@Ri

Function: Exchange Digit

Description: XCHD exchanges the low-order nibble of the Accumulator (bits 3-0), generally representing a hexadecimal or BCD digit, with that of the internal RAM location indirectly addressed by the specified register. The high-order nibbles (bits 7-4) of each register are not affected. No flags are affected.

Example: RO contains the address 20H. The Accumulator holds the value 36H (00l10110B). Internal RAM location 20H holds the value 75H (0111010lB). The instruction,

XCHD A,@R0

will leave RAM location 20H holding the value 76H (011101l0B) and 35H (00110101B) in the Accumulator.

Bytes: 1

Cycles: 1

Encoding:

1 1 0 1	0 1 1 i

Operation: XCHD

$$(A_{3\text{-}0}) \rightleftarrows ((Ri_{3\text{-}0}))$$

INSTRUCTION DEFINITIONS

XRL < dest-byte > , < src-byte >

Function: Logical Exclusive-OR for byte variables

Description: XRL performs the bitwise logical Exclusive-OR operation between the indicated variables, storing the results in the destination. No flags are affected.

The two operands allow six addressing mode combinations. When the destination is the Accumulator, the source can use register, direct, register-indirect, or immediate addressing; when the destination is a direct address, the source can be the Accumulator or immediate data.

(*Note*: When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, not the input pins.)

Example: If the Accumulator holds 0C3H (1100001 IB) and register 0 holds 0AAH (10101010B) then the instruction,

XRL A,R0

will leave the Accumulator holding the value 69H (01101001B).

When the destination is a directly addressed byte, this instruction can complement combinations of bits in any RAM location or hardware register. The pattern of bits to be complemented is then determined by a mask byte, either a constant contained in the instruction or a variable computed in the Accumulator at run-time. The instruction,

XRL PI, #00ll000lB

will complement bits 5, 4, and 0 of output Port 1.

INSTRUCTION DEFINITIONS

XRL A,Rn

Bytes: 1

Cycles: 1

Encoding:

0 1 1 0	1 r r r

Operation: XRL

$$(A) \leftarrow (A) \veebar (Rn)$$

XRL A,direct

Bytes: 2

Cycles: 1

Encoding:

0 1 1 0	0 1 0 1	direct address

Operation: XRL

$$(A) \leftarrow (A) \veebar (direct)$$

INSTRUCTION DEFINITIONS

XRL A,@Ri

Bytes: 1

Cycles: 1

0 1 1 0	0 1 1 i

Encoding:

Operation: XRL

$$(A) \leftarrow (A) \veebar ((Ri))$$

XRL A,#data

Bytes: 2

Cycles: 1

Encoding:

0 1 1 0	0 1 0 0	immediate data

Operation: XRL

$$(A) \leftarrow (A) \veebar \#data$$

INSTRUCTION DEFINITIONS

<u>**XRL direct,A**</u>

Bytes: 2

Cycles: 1

Encoding:

0 1 1 0	0 0 1 0	direct address

Operation: XRL

$$(\text{direct}) \leftarrow (\text{direct}) \veebar (A)$$

<u>**XRL direct,#data**</u>

Bytes: 3

Cycles: 2

Encoding:

0 1 1 0	0 0 1 1	direct address	immediate data

Operation: XRL

$$(\text{direct}) \leftarrow (\text{direct}) \veebar \#\text{data}$$