Power Converter Systems

Graduate Course EE8407

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Ryerson Campus

Topic 6

Multilevel Cascaded H-Bride (CHB) Inverters

H-bride power cells

CHB Inverter Fed Drive Source: Toshiba - General Electric

Multilevel CHB Inverters

Lecture Topics

- H-Bridge Inverter
- CHB Inverter Topologies
- Phase Shifted PWM
- Level Shifted PWM
- PWM Scheme Comparison

Multilevel CHB Inverters

Why Use Multilevel Inverters?

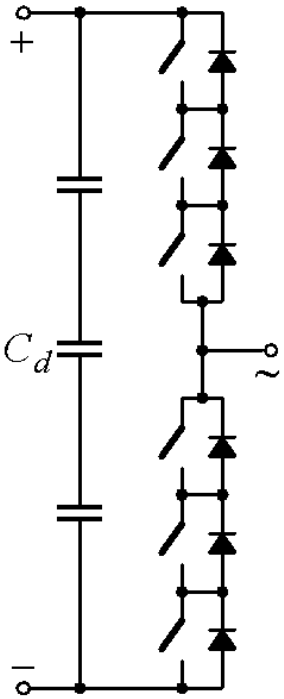
- To increase inverter operating voltage without devices in series
- To minimize THD with low switching frequencies f_{sw}
- To reduce EMI due to lower voltage steps

Switching frequency for high power converters:

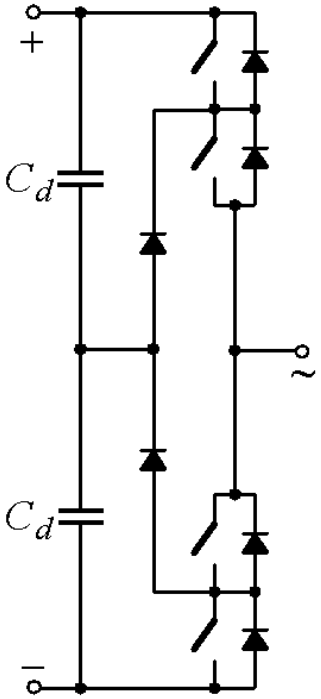
f_{sw} = 60Hz ~ 1000Hz

Multilevel Inverter Topologies

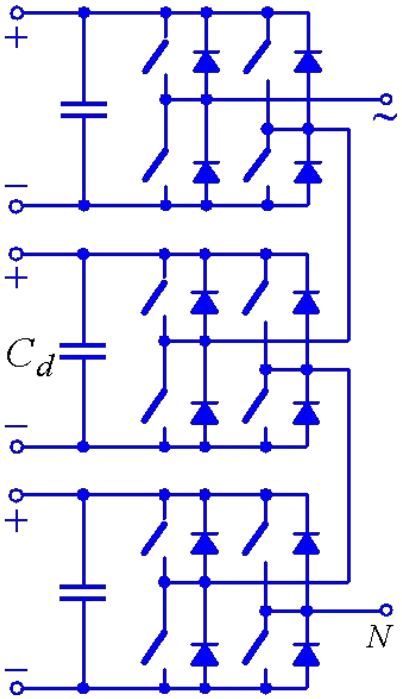
- **Per-Phase Diagram**



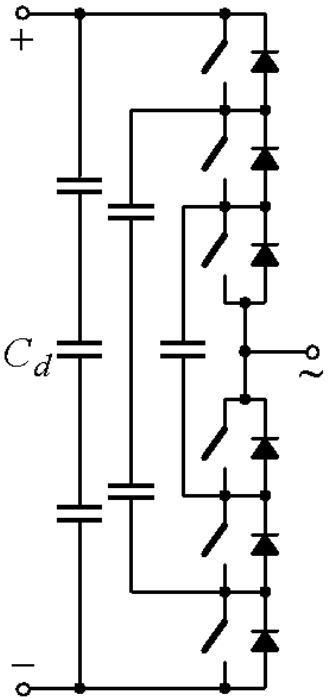
Two Level Inverter



Neutral Point Clamped (NPC) Inverter



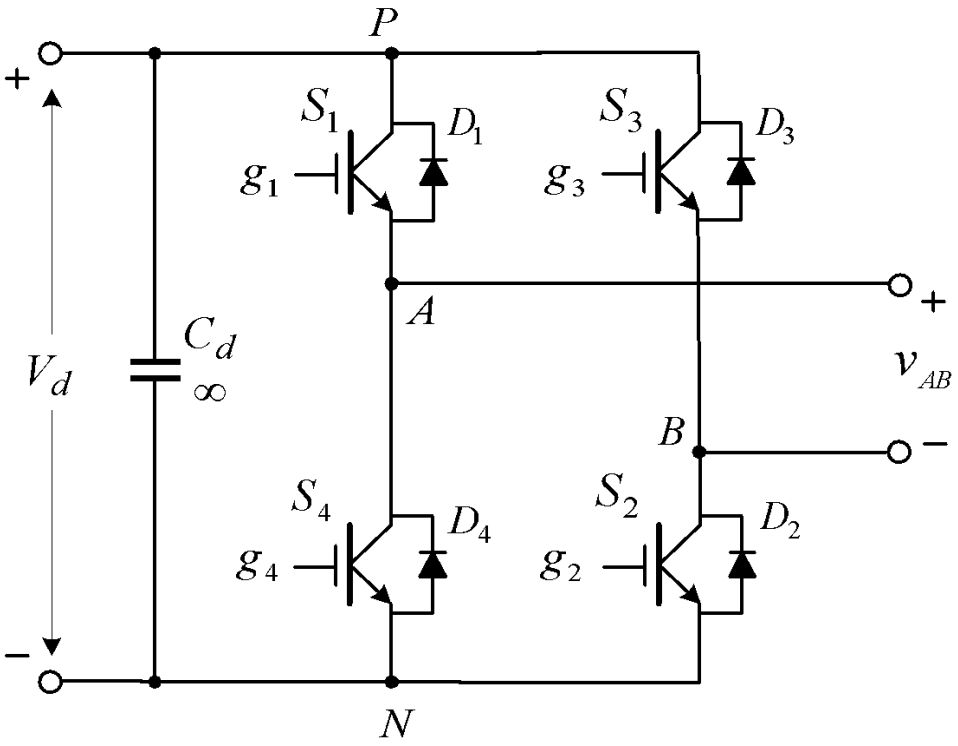
Cascaded H-bridge (CHB) Inverter



Flying Capacitor Inverter

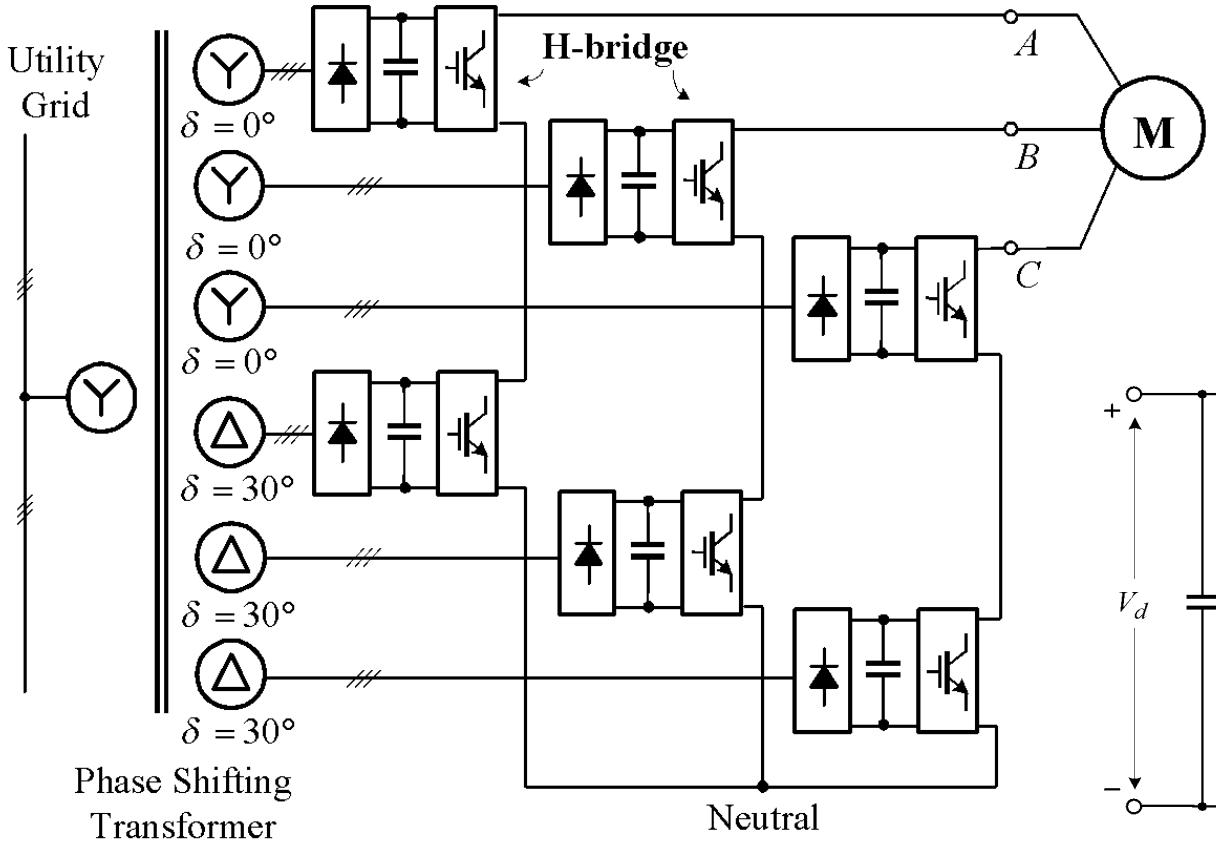
H-Bridge Inverter

- H-bridge Power Cell

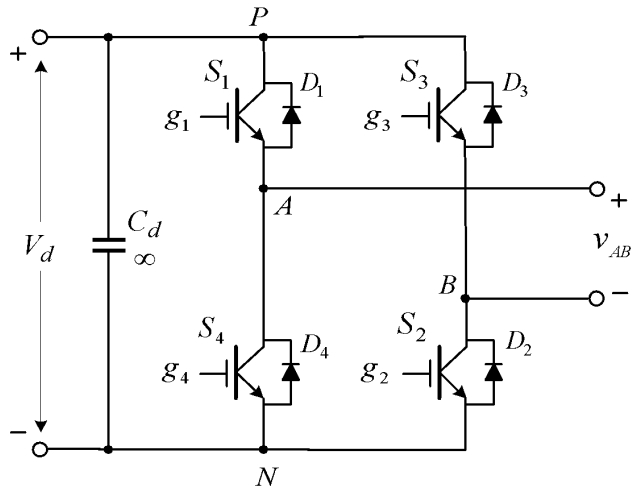


H-Bridge Inverter

- **Typical Industrial Applications**



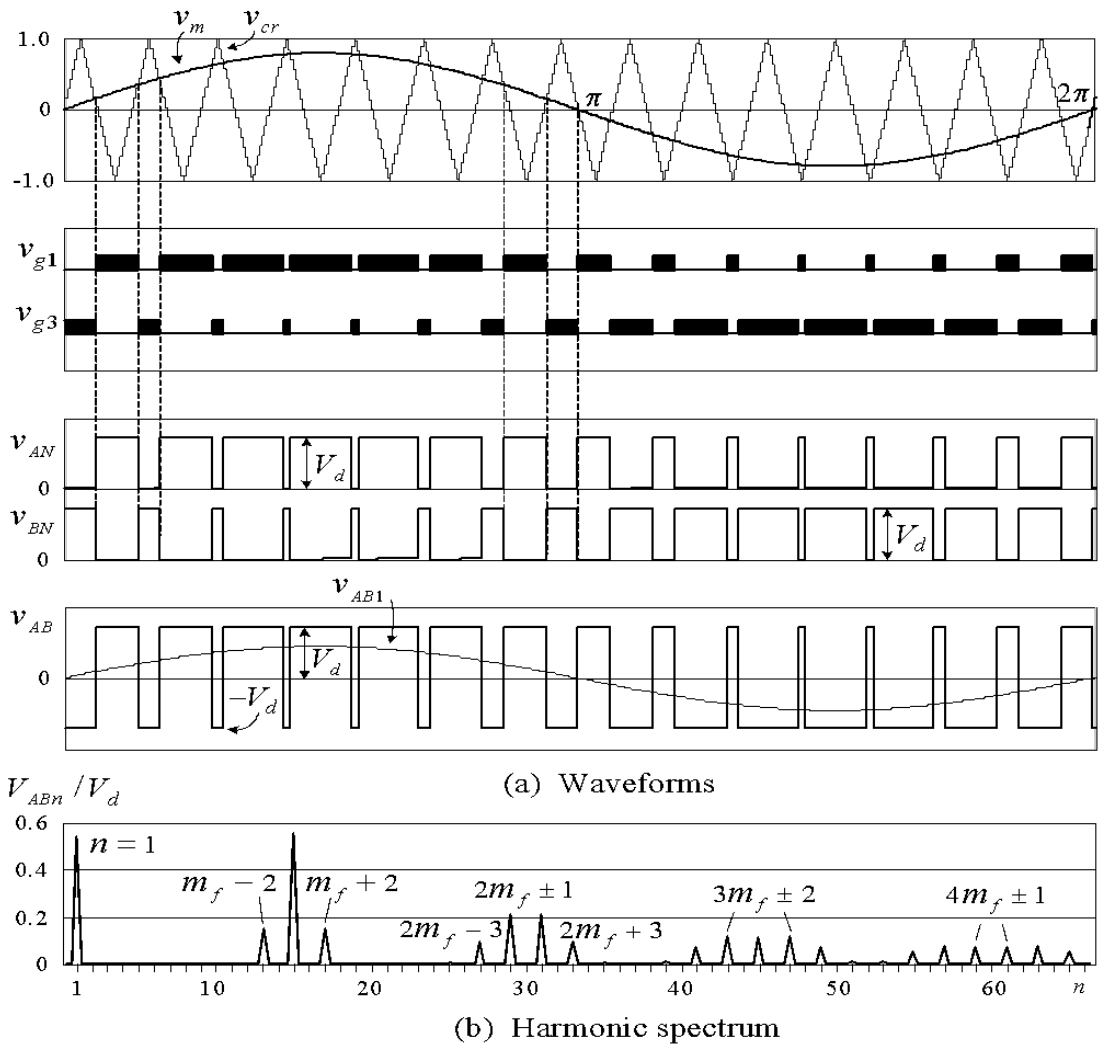
Five-level CHB inverter

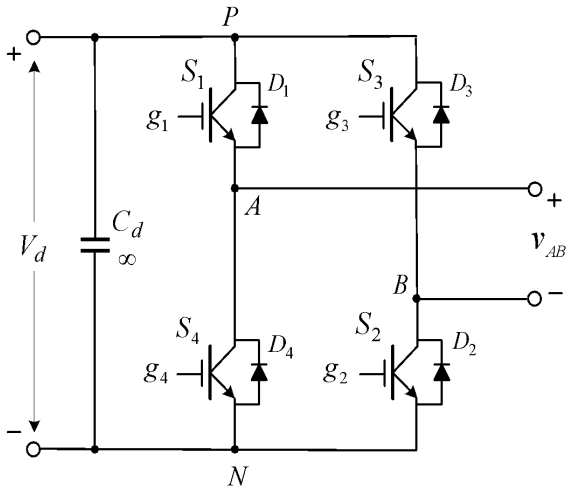


H-bridge Power Cell

H-Bridge Inverter

- **Bipolar Modulation**



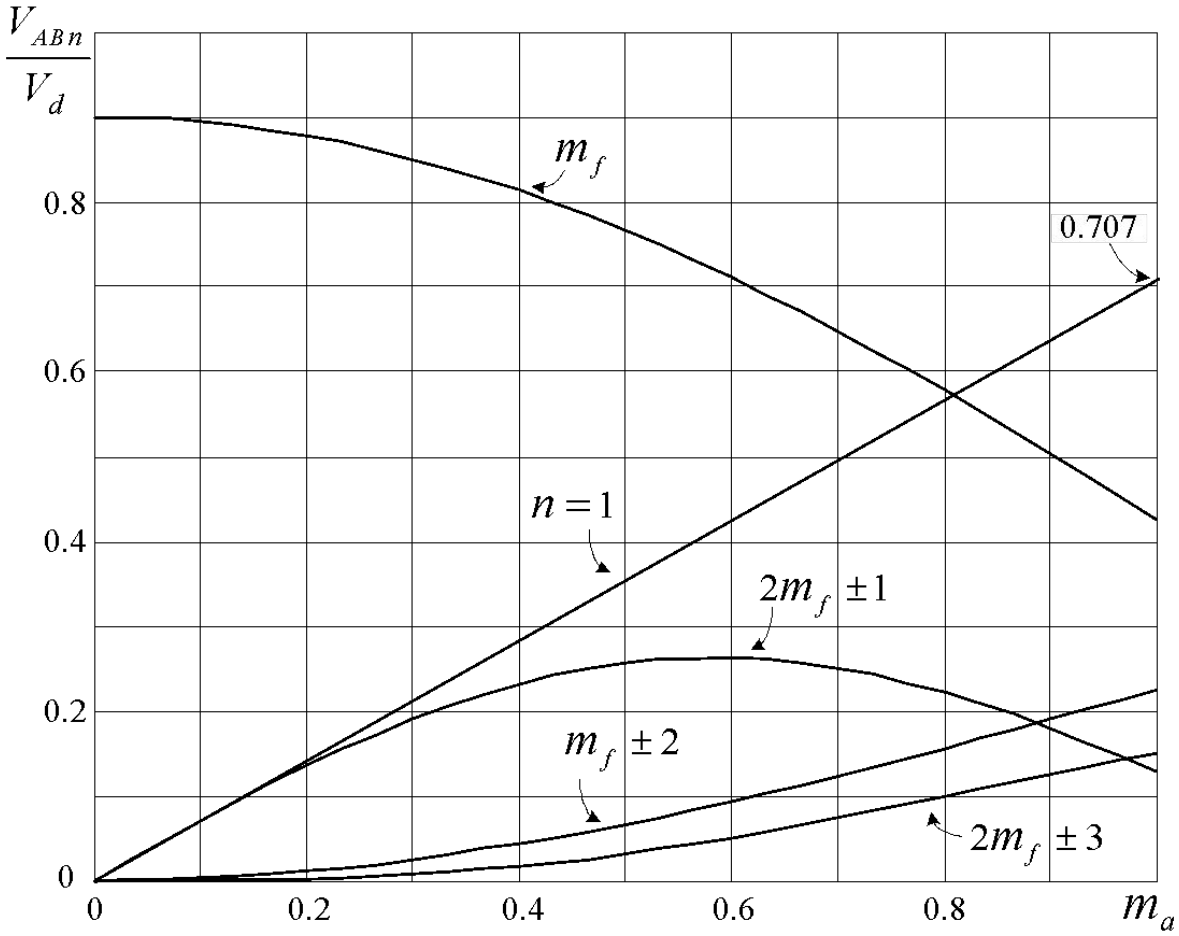


Bipolar PWM:

V_{AB} from $-V_d$ to $+V_d$ or from $+V_d$ to $-V_d$

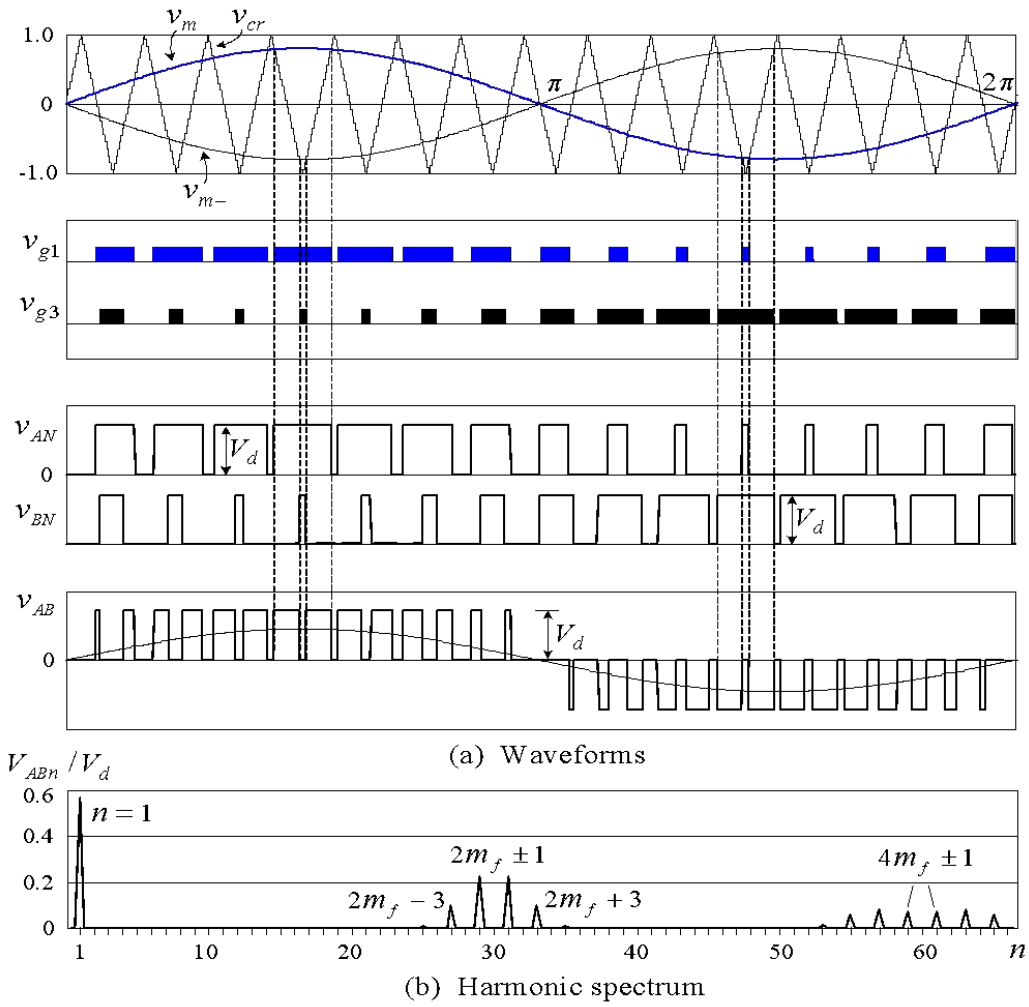
H-Bridge Inverter

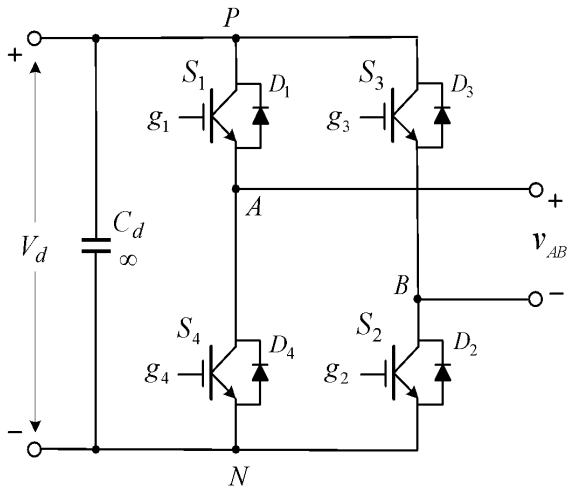
- **Bipolar Modulation (FFT)**



H-Bridge Inverter

- **Unipolar Modulation (1)**





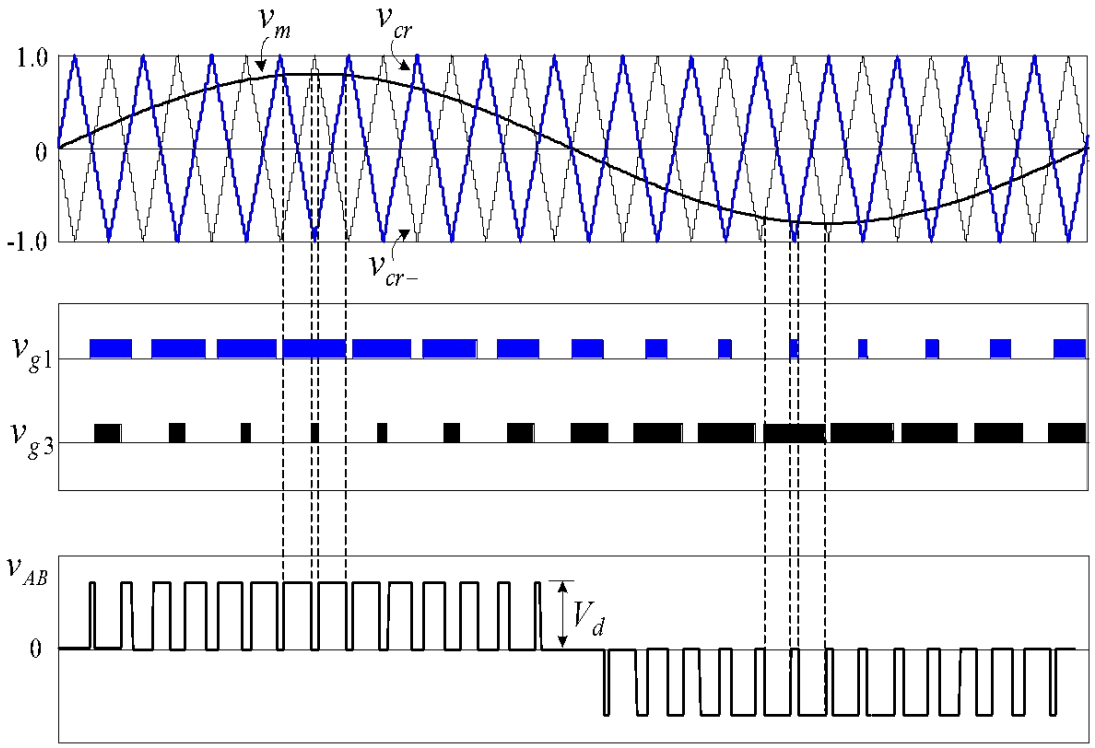
- **Two modulation waves V_m and V_{m-}**
- **One carrier wave V_{cr}**

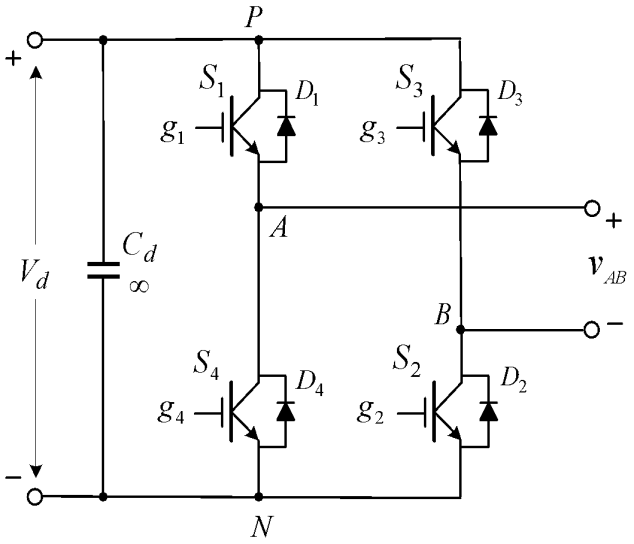
- **Unipolar PWM:**

  V_{AB} from 0 to $+V_d$ or from 0 to $-V_d$

H-Bridge Inverter

- **Unipolar Modulation (2)**

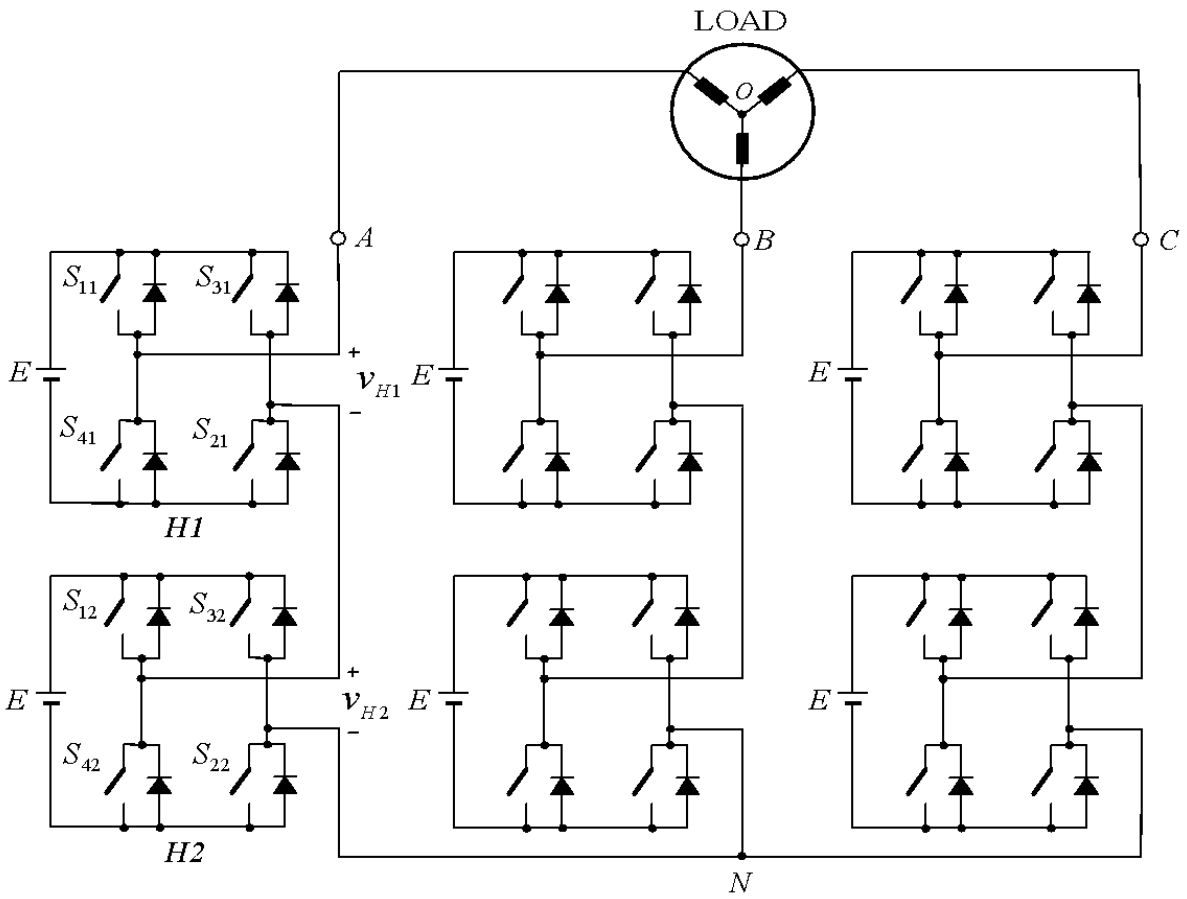




- One modulating wave: V_m
- Two carrier waves: V_{cr} and V_{cr-}

CHB Inverter Topologies

- **Five-Level CHB Inverter**



Complementary Switch pairs:

S_{11} and S_{41};
S_{31} and S_{21};

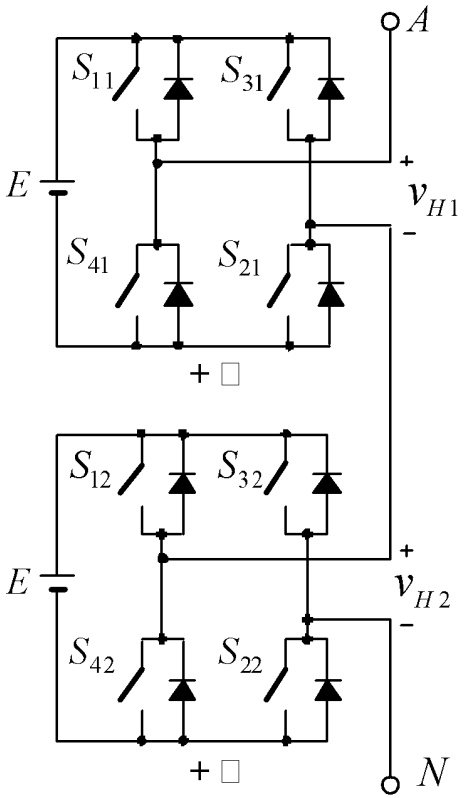
S_{12} and S_{42};
S_{32} and S_{22};

Converters in cascade, but no switching devices in series.

CHB Inverter Topologies

- **Output Voltage and Switching Status** (five-level)

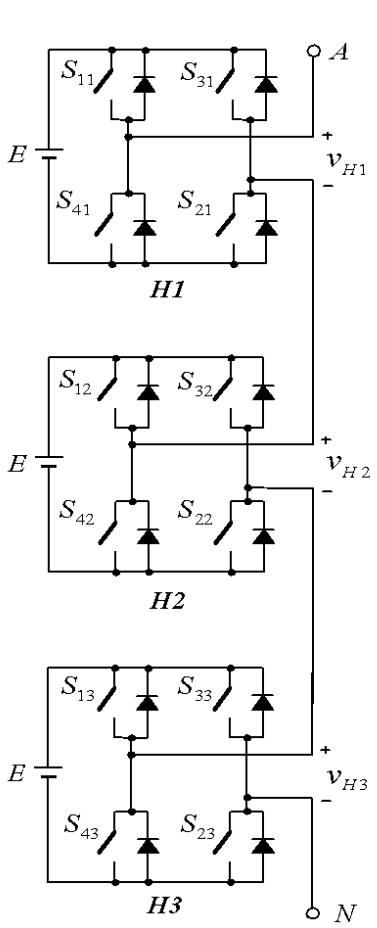
Output Voltage v_{AN}	Switching State S_{11}	S_{31}	S_{12}	S_{32}	v_{H1}	v_{H2}
2E	1	0	1	0	E	E
E	1	0	1	1	E	0
	1	0	0	0	E	0
	1	1	1	0	0	E
	0	0	1	0	0	E
0	0	0	0	0	0	0
	0	0	1	1	0	0
	1	1	0	0	0	0
	1	1	1	1	0	0
	1	0	0	1	E	-E
	0	1	1	0	-E	E
-E	0	1	1	1	-E	0
	0	1	0	0	-E	0
	1	1	0	1	0	-E
	0	0	0	1	0	-E
-2E	0	1	0	1	-E	-E



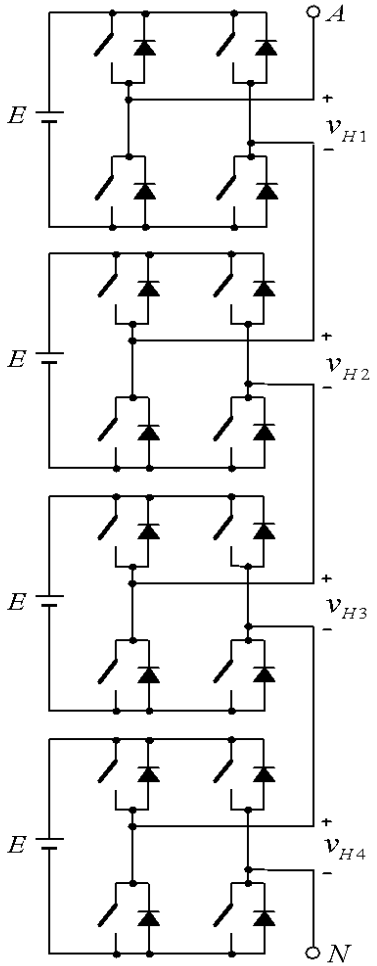
Waveform of V_{AN} is composed of five voltage levels: *2E*, *E*, 0, *-E*, and *-2E*

CHB Inverter Topologies

- **Seven- and Nine-Level Inverters (Per phase diagram)**



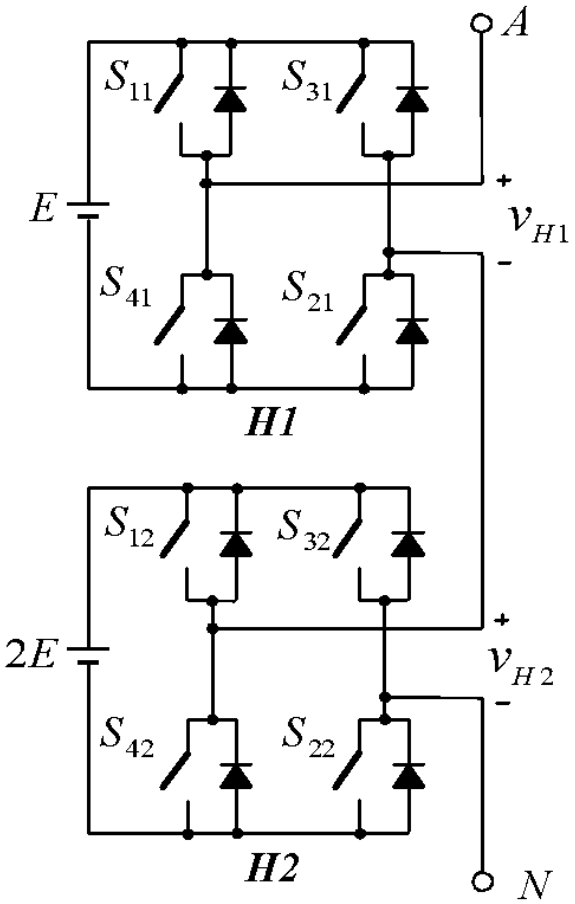
(a) Seven-level inverter



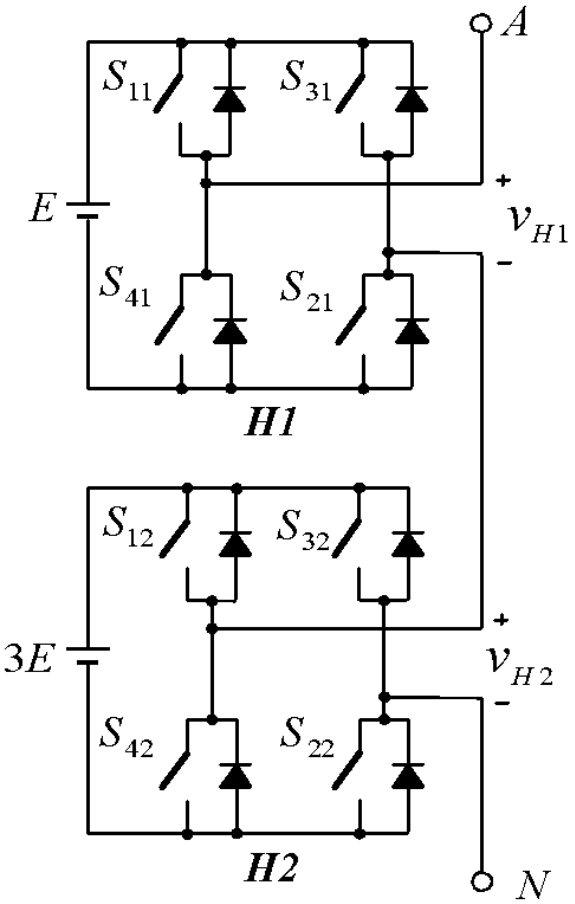
(b) Nine-level inverter

CHB Inverter Topologies

- **Unequal dc Bus Voltages**



(a) Two-cell seven-level topology

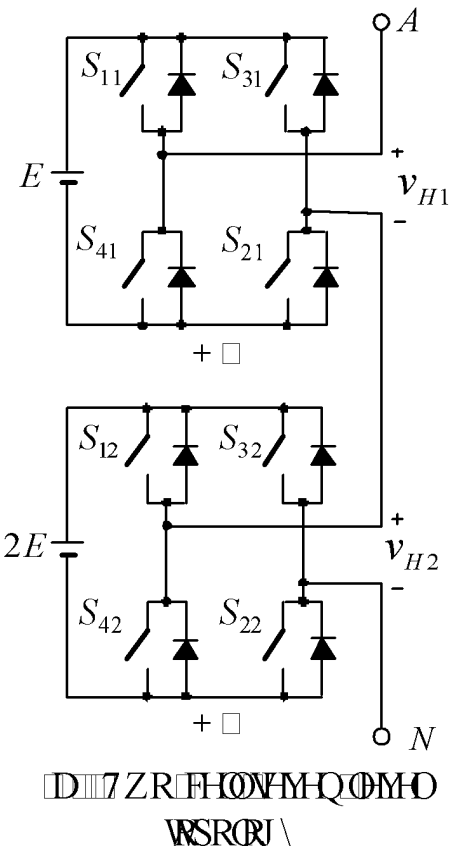


(b) Two-cell nine-level topology

CHB Inverter Topologies

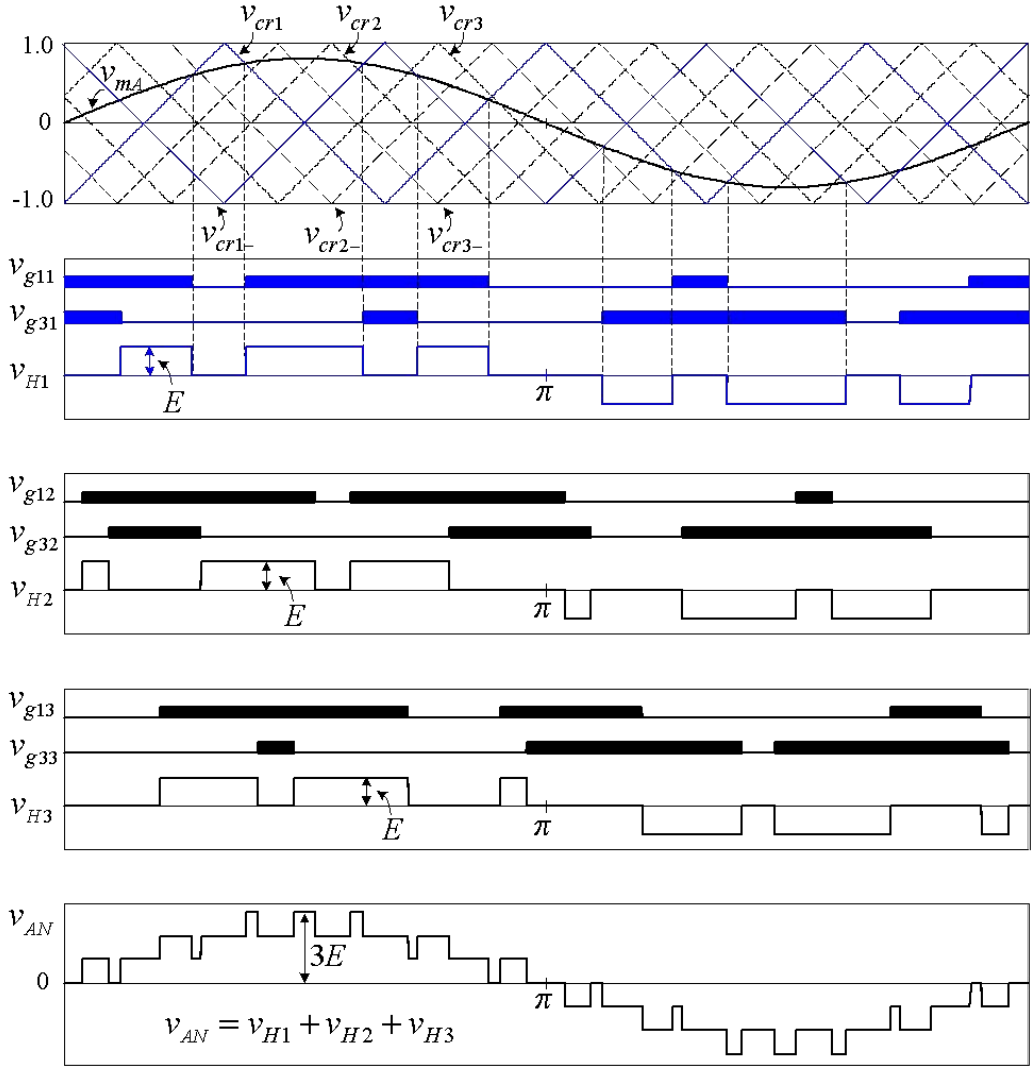
- **Unequal dc Bus Voltages (Two-cell seven-level topology)**

Output Voltage V_{AN}	Switching State				V_{H1}	V_{H2}
	S_{11}	S_{31}	S_{12}	S_{32}		
3*E*	1	0	1	0	*E*	*2E*
2*E*	1	1	1	0	*0*	*2E*
	0	0	1	0	*0*	*2E*
E	1	0	1	1	*E*	*0*
	1	0	0	0	*E*	*0*
	0	1	1	0	*-E*	*2E*
0	0	0	0	0	*0*	*0*
	0	0	1	1	*0*	*0*
	1	1	0	0	*0*	*0*
	1	1	1	1	*0*	*0*
-E	1	0	0	1	*E*	*-2E*
	0	1	1	1	*-E*	*0*
	0	1	0	0	*-E*	*0*
-2*E*	1	1	0	1	*0*	*-2E*
	0	0	0	1	*0*	*-2E*
-3*E*	0	1	0	1	*-E*	*-2E*



Phase Shifted PWM

- **Carrier Based PWM – Phase Shifted**



- # of voltage levels: $m = 7$
- # of carriers: $m_c = m - 1 = 6$
- Phase shift: 360° / m_c = 60°

Carriers for *H1* bridge: v_{cr1} and v_{cr1-}

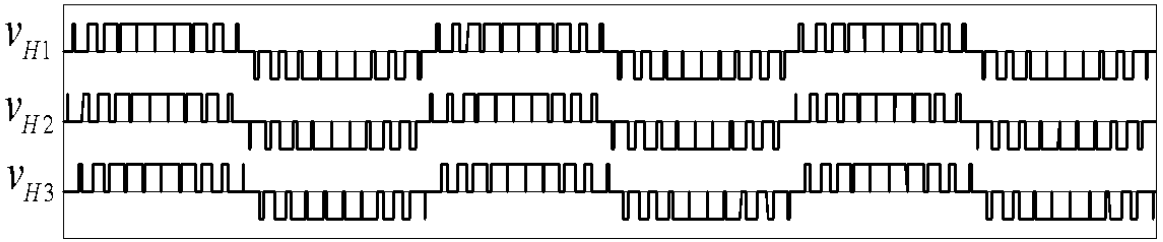
Carriers for *H2* bridge: v_{cr2} and v_{cr2-}

Carriers for *H3* bridge: v_{cr3} and v_{cr3-}

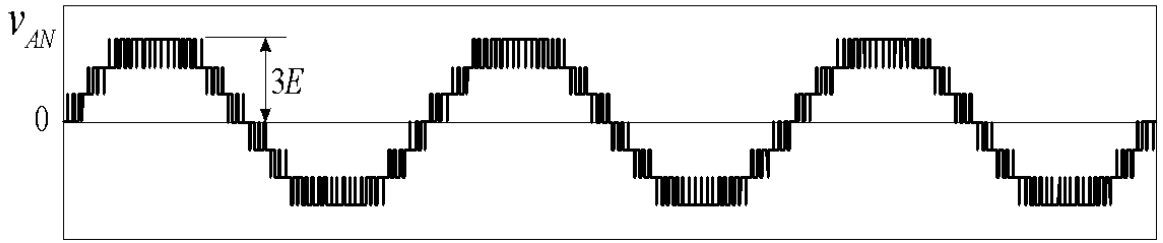
$m = 7$

Phase Shifted PWM

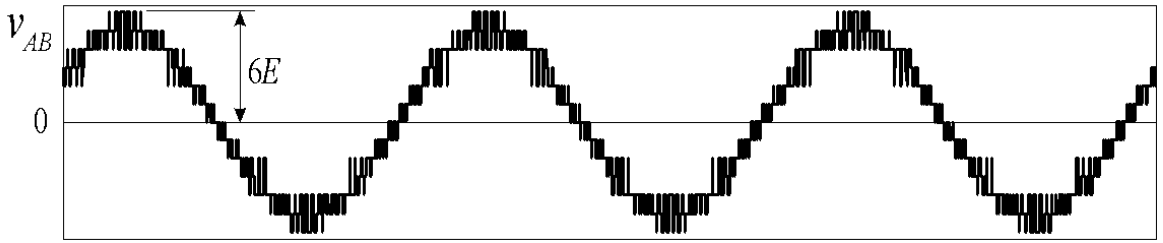
- **Inverter Waveforms** (7-level, phase shifted)



- Switching occurs at different times
- $f_{sw(device)} = 60\ m_f = 600\text{Hz}$



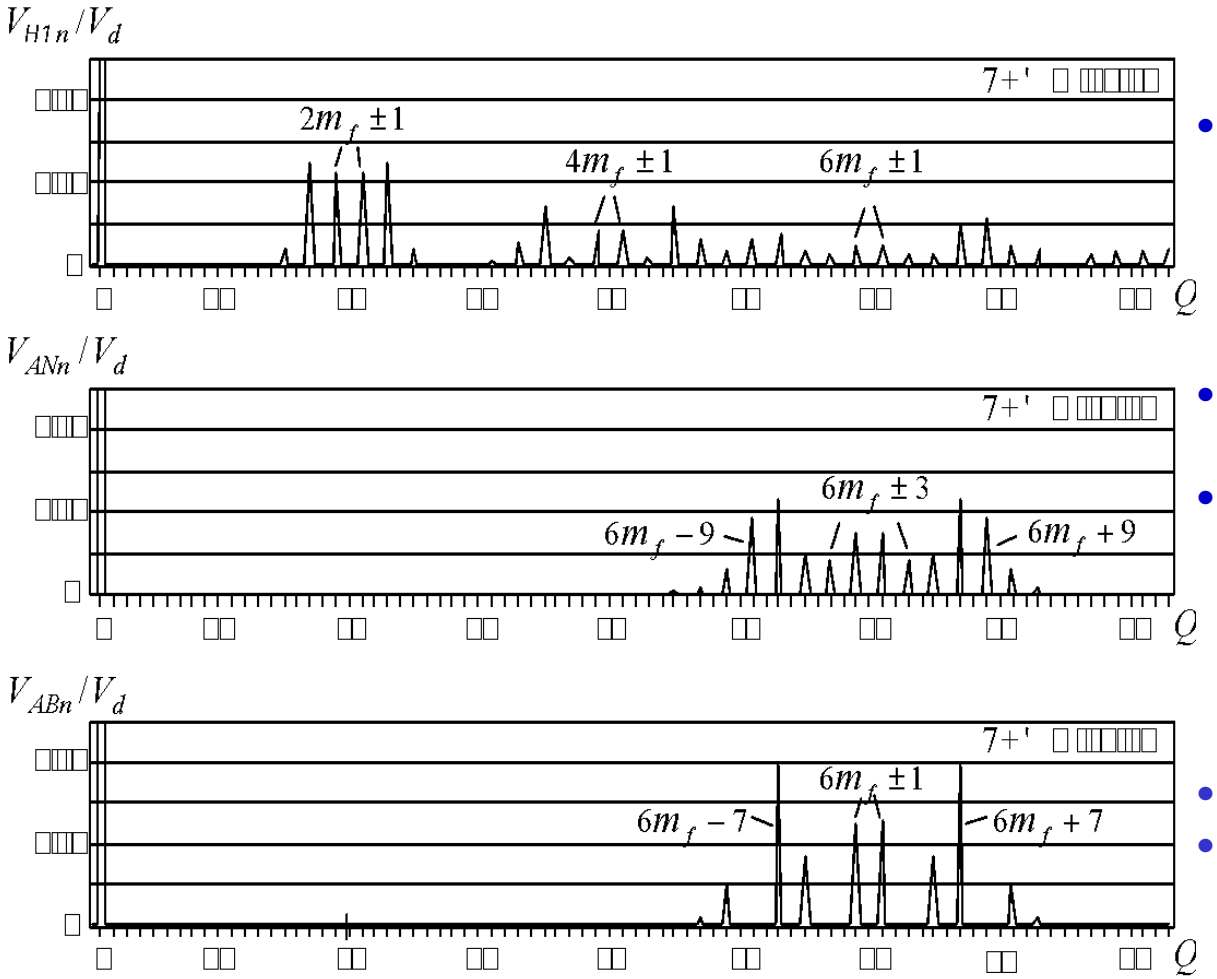
- Inverter phase voltage levels: 7
- Low EMI



- Line-to-line voltage levels: 13
- Close to a sinusoid
- Low THD

Phase Shifted PWM

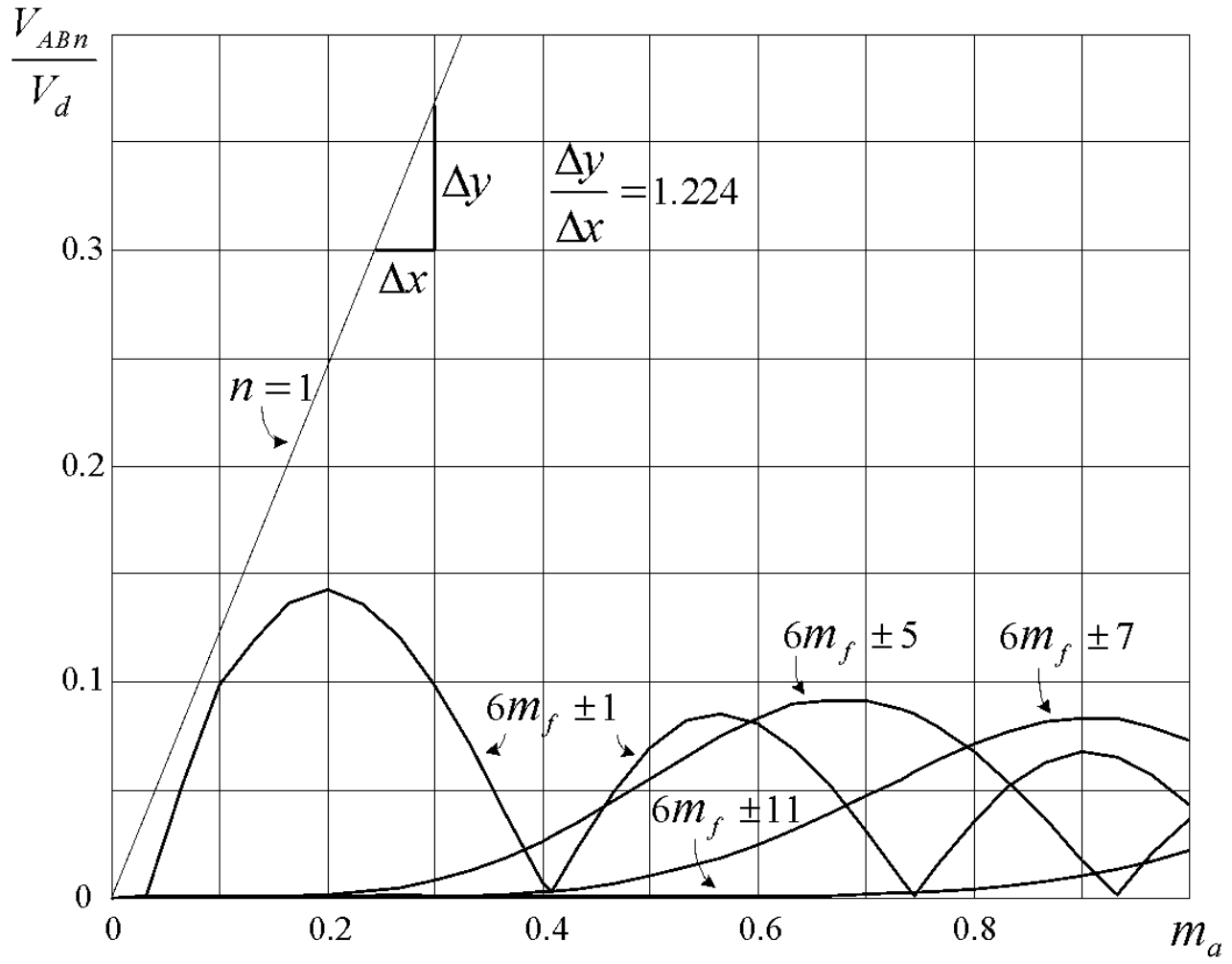
- **FFT** (7-level, phase shifted)



- **Lowest harmonics: around $2m_f$**
- **Lowest harmonics: around $6m_f$**
- **Containing triplen harmonics**
- **No triplen harmonics**
- **Equivalent $f_{sw(inverter)}$ = 60($6m_f$) = 3600Hz**

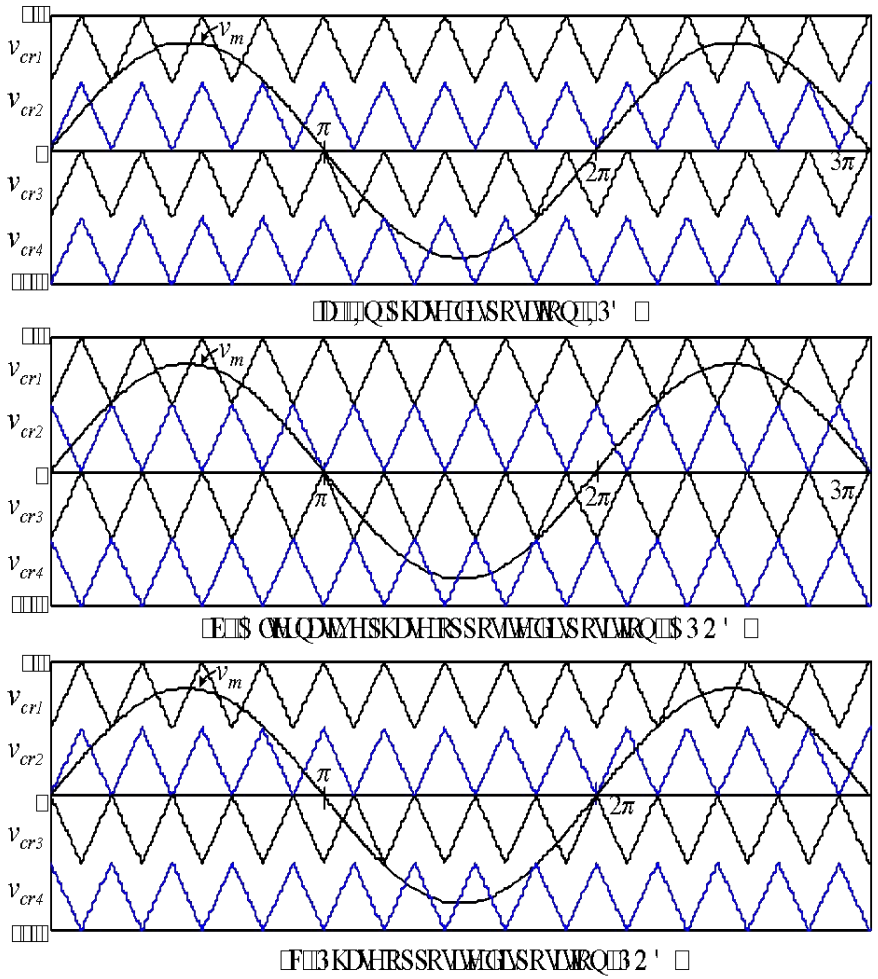
Phase Shifted PWM

- **Harmonic Content** (7-level, phase shifted)



Level Shifted PWM

- **Carrier Based PWM – Level Shifted**



IPD

APOD

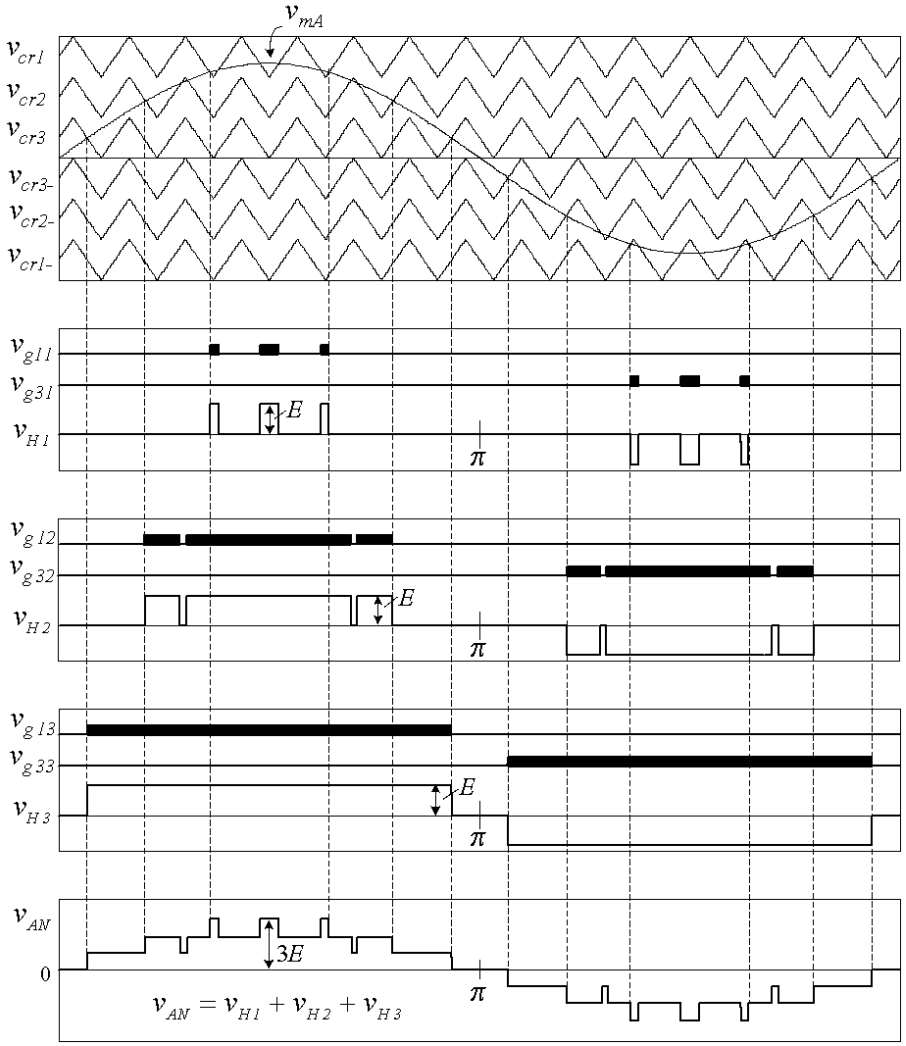
POD

- **# of voltage levels:**
  $m = 5$
- **# of carriers:**
  $m_c = m - 1 = 4$

IPD provides the best harmonic profile.

Level Shifted PWM

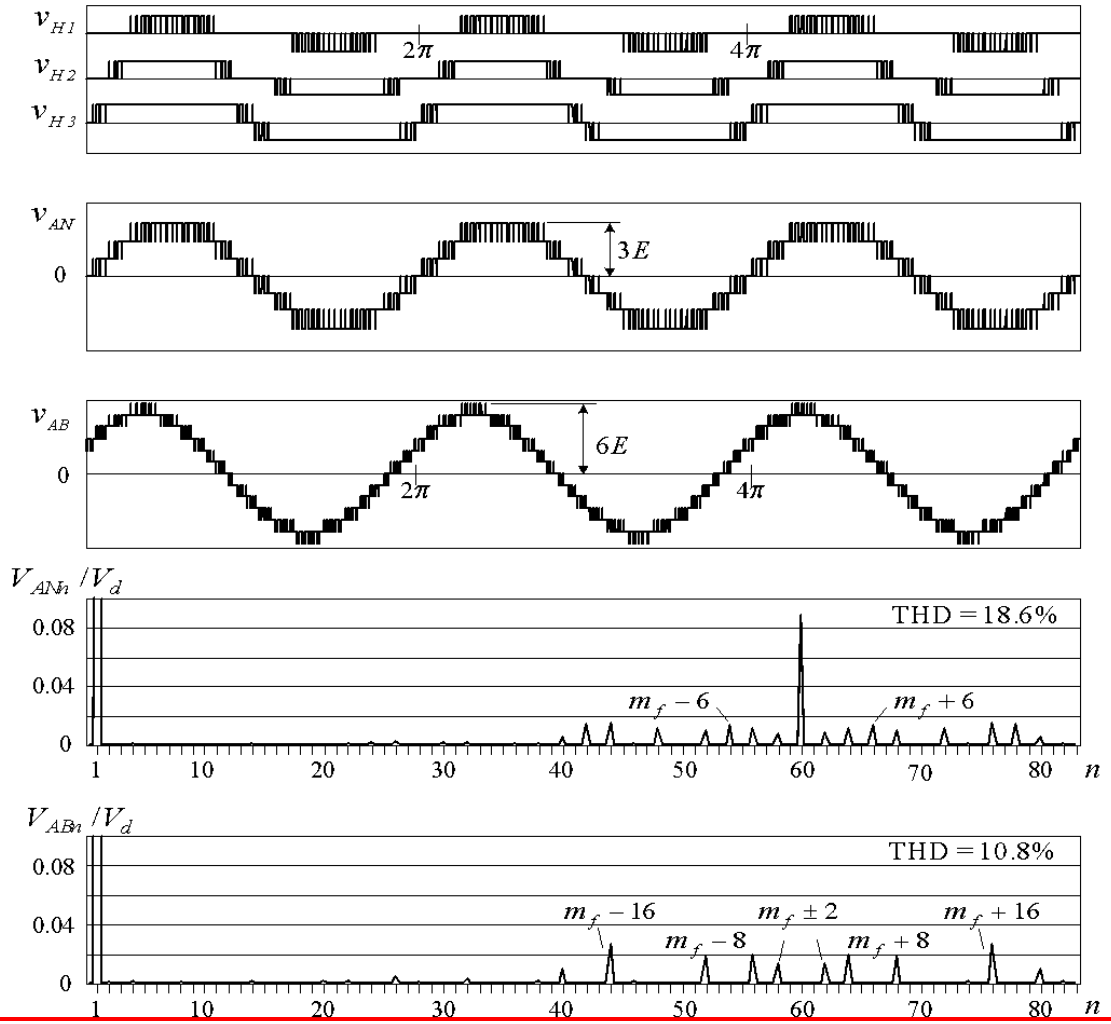
- **Gating Arrangement** (7-level)



- # of voltage levels:
  $m = 7$
- # of carriers:
  $m_c = m - 1 = 6$
- $f_{sw(device)}$:
  - not equal to f_{cr}, and
  - not the same for all switches.
- Device conduction angle:
  - not equal.
- Necessary to swap switching pattern.

Level Shifted PWM

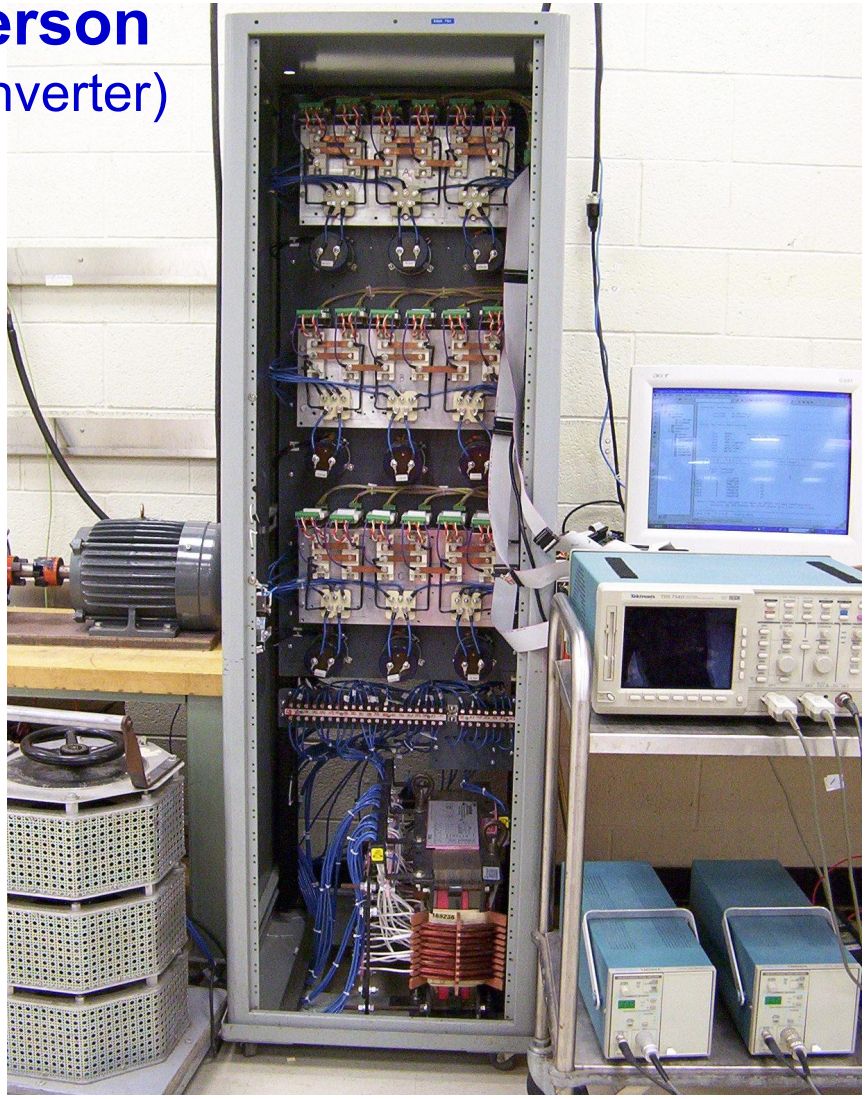
- **Inverter Output Voltages** (seven-level)



- $m = 7$
- Switching occurs at different times
- $f_{sw(device)} = f_{cr}/m_c =$ 600Hz (avg)
- v_{AB} close to a sinusoid
- Low THD, low EMI
- $f_{sw(inv)} = f_c = 3600$Hz

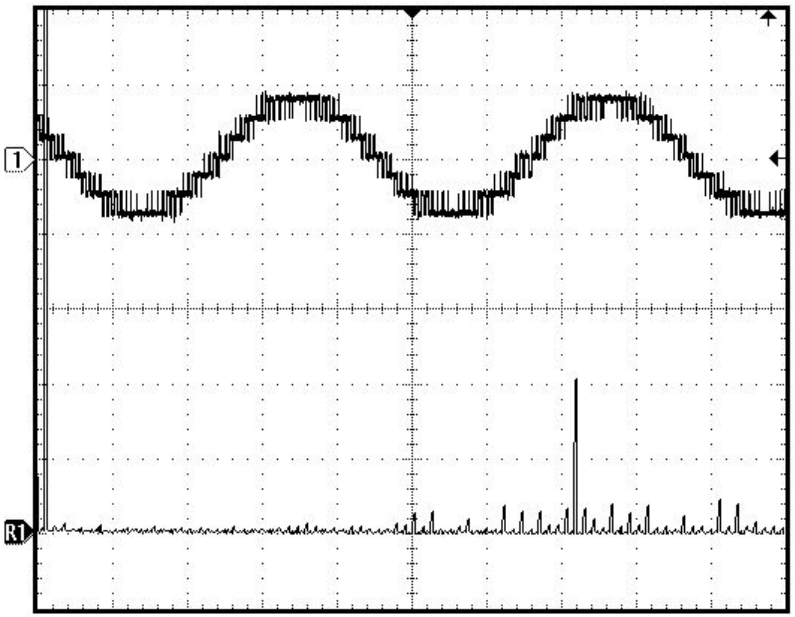
Level Shifted PWM

- **Prototype at Ryerson**
  (Seven-level CHB Inverter)

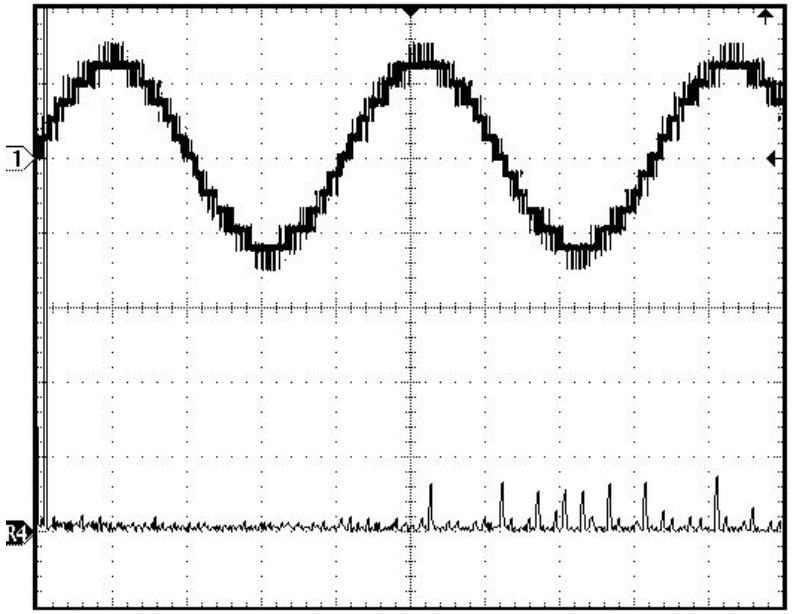


Level Shifted PWM

- **Measured Waveforms** (IPD, 7-level)



Inverter phase voltage V_{AZ}



Line-to-line voltage V_{AB}

PWM Scheme Comparison

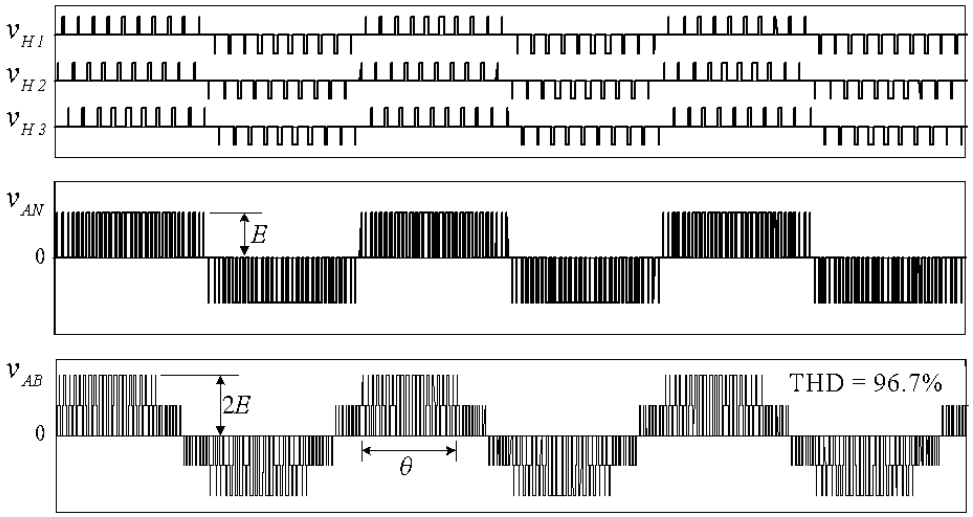
- PWM at Low m_a

- At m_a = 0.2:
  - Phase shifted PWM:

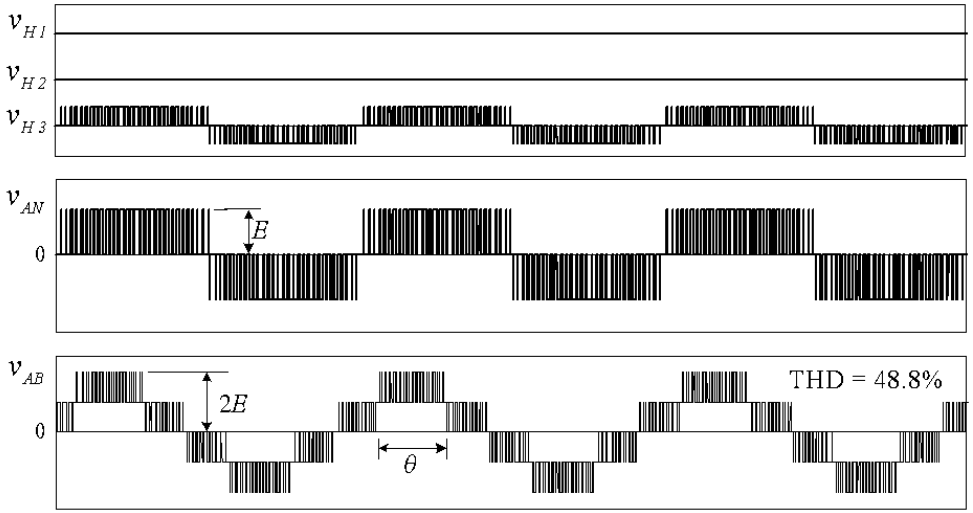
    THD = 96.7%

  - Level shifted PWM:

    THD = 48.8%



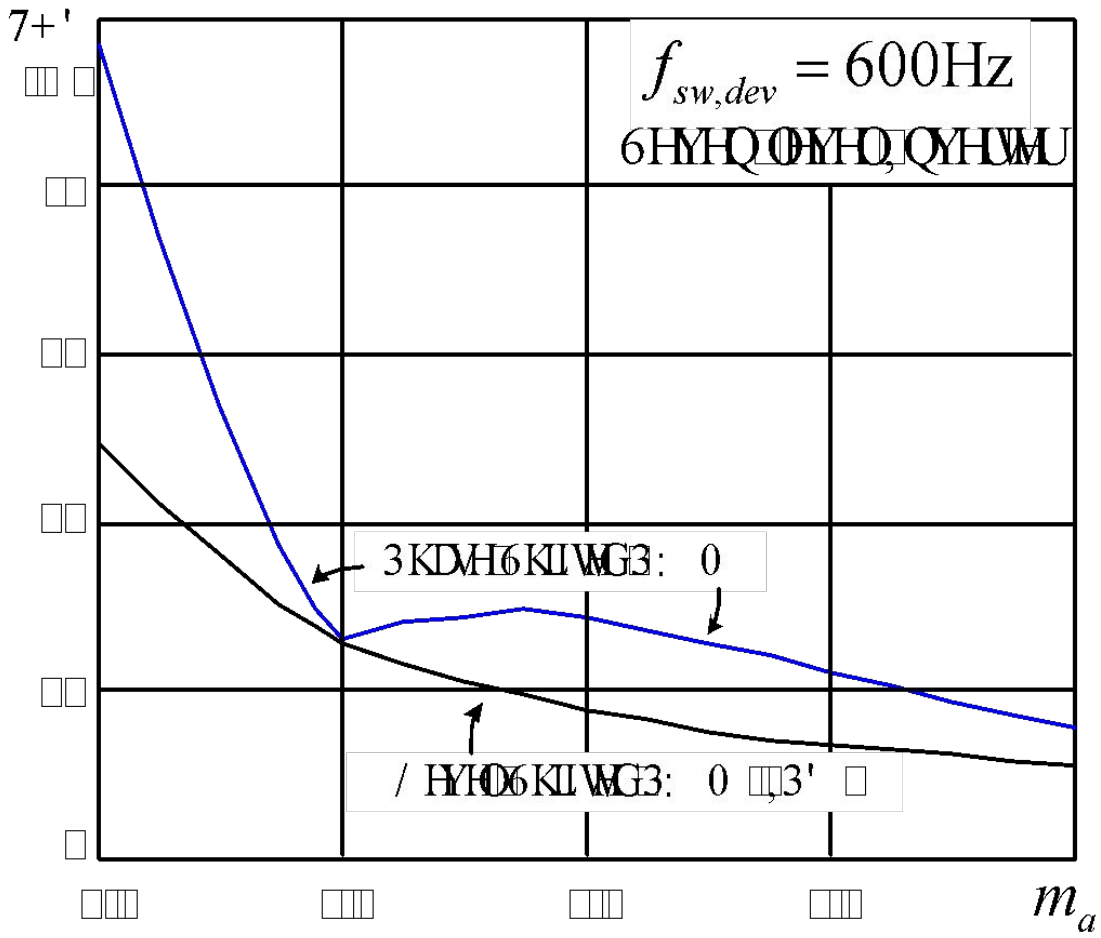
(a) Phase-shifted modulation



(b) Level-shifted modulation (IPD)

PWM Scheme Comparison

- Total Harmonic Distortion (THD)



PWM Scheme Comparison

- **Summary**

Comparison	Phase-shifted Modulation	Level-shifted Modulation (IPD)
Device Switching Frequency	Same for all devices	Different
Device Conduction Period	Same for all devices	Different
Rotating of switching patterns	No required	Required
THD of inverter output line-to-line voltage	Good	Better
Low Order Harmonics	No	Yes (Very low amplitude)

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Thanks