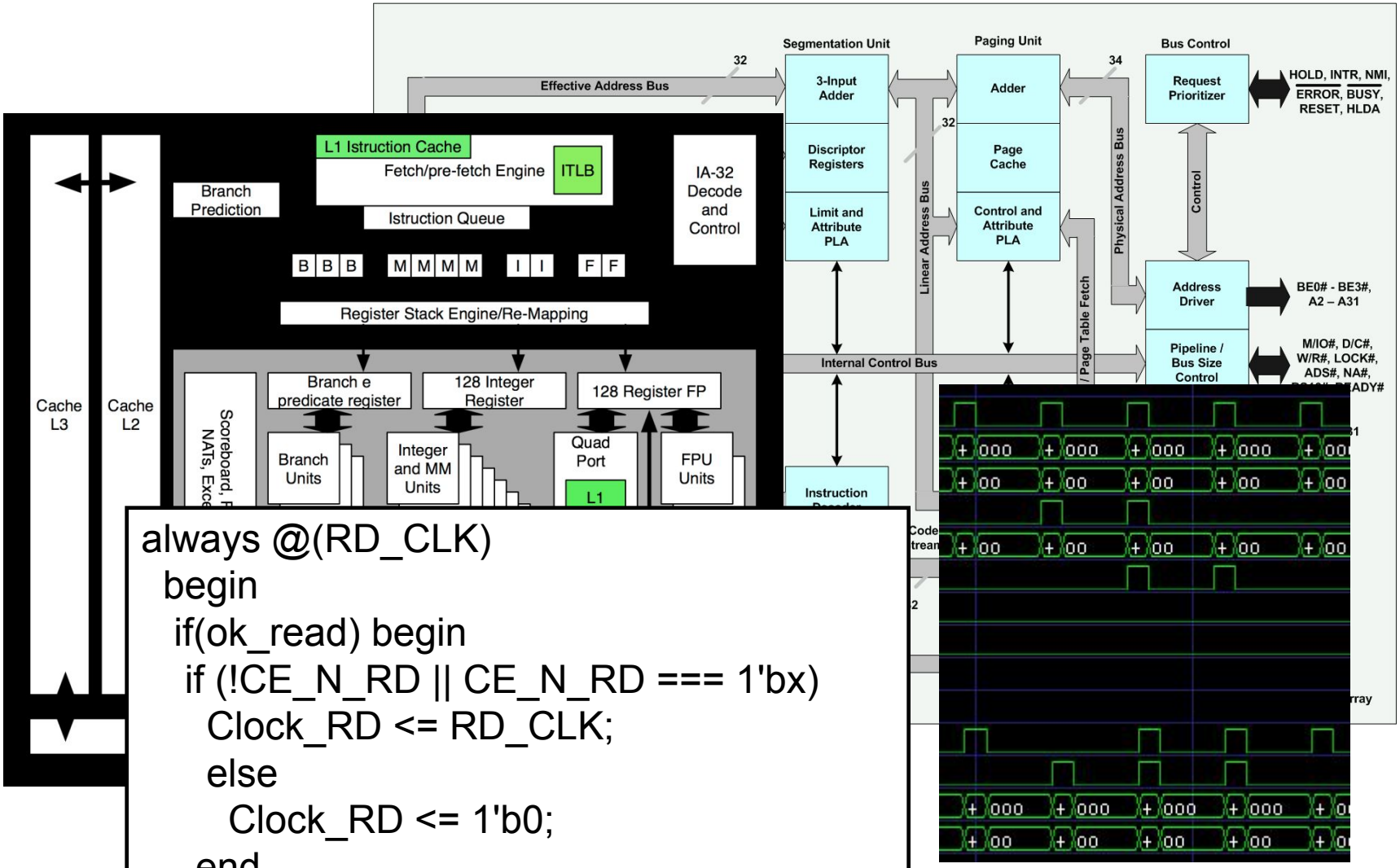
Модели аппаратуры




```
always @(RD_CLK)
  begin
   if(ok_read) begin
    if (!CE_N_RD || CE_N_RD === 1'bx)
      Clock_RD <= RD_CLK;
      else
        Clock_RD <= 1'b0;
     end
   end
```

Верификация моделей аппаратуры

- Верификация и тестирование занимает до 70% времени разработки:
  - проверяются алгоритмы;
  - проверяется кодирование алгоритмов;
  - проверяется соединение блоков и т.д.

Пример ошибки

div r1, r2 → Lo, Hi

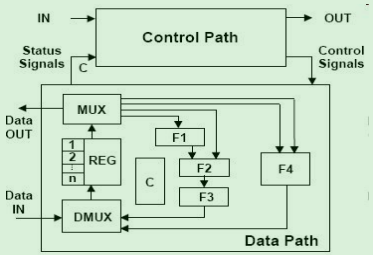
mthi r3 → Hi

mfhi r4

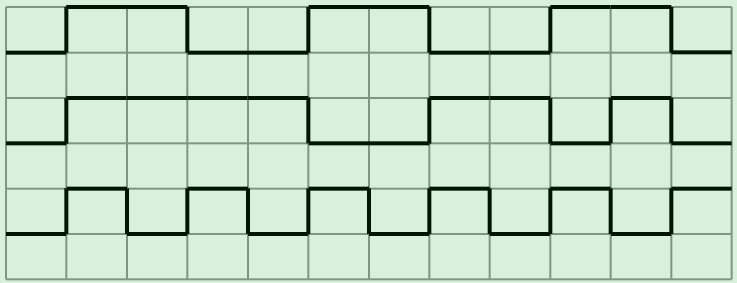
Уровни верификации микропроцессоров

Модульный уровень

Тестируется модель отдельного модуля

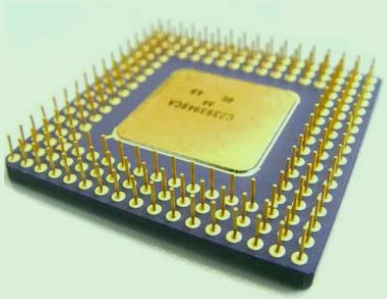


через входные и выходные сигналы



Системный уровень

Модель микропроцессора тестируется целиком



с помощью тестовых программ

```
lui  s1, 0xdead
ori  s1, s1, 0x0
lui  s3, 0xbeef
ori  s3, s3, 0xf
add  v0, a0, a2
sub  t1, t3, t5
add  t7, s1, s3
```

Инструментальная поддержка

MicroTESK - Komdiv64 Test Program Generator - <Unknown>.section

File Generation Window Help

S T W

Komdiv64
- cp1
  - arithmetic
    - abs.s
      - Random
    - abs.d
    - abs.ps
    - addsub.ps
    - add.s
    - add.d
    - add.ps
    - div.s
    - div.d
    - madd.s
    - madd.d
    - madd.ps
    - maddsub1.ps
    - maddsub2.ps
    - msub.s
    - msub.d
    - msub.ps
    - mul.s
    - mul.d
    - mul.ps
    - neg.s
    - neg.d
    - neg.ps
    - nmadd.s
    - nmadd.d
    - nmadd.ps
    - nmsub.s
    - nmsub.d
    - nmsub.ps
    - recip.s

<Unknown>
- section

Group ARITHMETIC (cp1.arithmetic)

Test	Subgroup or Instruction	Equivalence Class	Situations
	abs.s	ABS_Equivalence_Class	1/1
	abs.d	ABS_Equivalence_Class	1/1
	abs.ps	ABS_Equivalence_Class	1/1
	addsub.ps	ADD_Equivalence_Class	1/1
	add.s	ADD_Equivalence_Class	1/1
	add.d	ADD_Equivalence_Class	1/1
	add.ps	ADD_Equivalence_Class	1/1
	div.s	DIV_Equivalence_Class	1/1
	div.d	DIV_Equivalence_Class	1/1
	madd.s	MADD_Equivalence_Class	1/1
	madd.d	MADD_Equivalence_Class	1/1
	madd.ps	MADD_Equivalence_Class	1/1
	maddsub1.ps	MADD_Equivalence_Class	1/1
	maddsub2.ps	MADD_Equivalence_Class	1/1
	msub.s	MADD_Equivalence_Class	1/1
	msub.d	MADD_Equivalence_Class	1/1
	msub.ps	MADD_Equivalence_Class	1/1
	mul.s	MUL_Equivalence_Class	1/1
	mul.d	MUL_Equivalence_Class	1/1
	mul.ps	MUL_Equivalence_Class	1/1
	neg.s	NEG_EquivalenceClass	1/1
	neg.d	NEG_EquivalenceClass	1/1
	neg.ps	NEG_EquivalenceClass	1/1
	nmadd.s	MADD_Equivalence_Class	1/1
	nmadd.d	MADD_Equivalence_Class	1/1
	nmadd.ps	MADD_Equivalence_Class	1/1
	nmsub.s	MADD_Equivalence_Class	1/1
	nmsub.d	MADD_Equivalence_Class	1/1
	nmsub.ps	MADD_Equivalence_Class	1/1
	recip.s	RECIP_Equivalence_Class	1/1

Top Groups: 0/0 (100%) Leaf Groups: 0/0 (100%) Instructions: 38/38 (100%) Situations: 38/38 (100%)

Generator Console

```
Generating file: test_00000.S
Creating package: test_00000
Moving file: test_00000.S to C:\Documents and Settings\root\Desktop\tests\test_00000
Generating file: test_00001.S
Creating package: test_00001
Moving file: test_00001.S to C:\Documents and Settings\root\Desktop\tests\test_00001
Generating file: test_00002.S
Creating package: test_00002
Moving file: test_00002.S to C:\Documents and Settings\root\Desktop\tests\test_00002
```

Top Groups: 0/0 (100%) Leaf Groups: 11/11 (100%) Instructions: 191/191 (100%) Situations: 191/191 (100%)