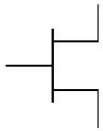
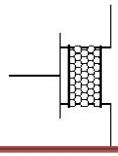
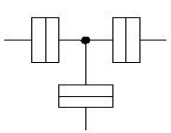
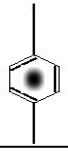
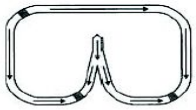
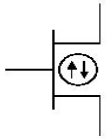
Институт физики полупроводников СО РАН, Новосибирск

КМОП технология вблизи физических пределов масштабирования

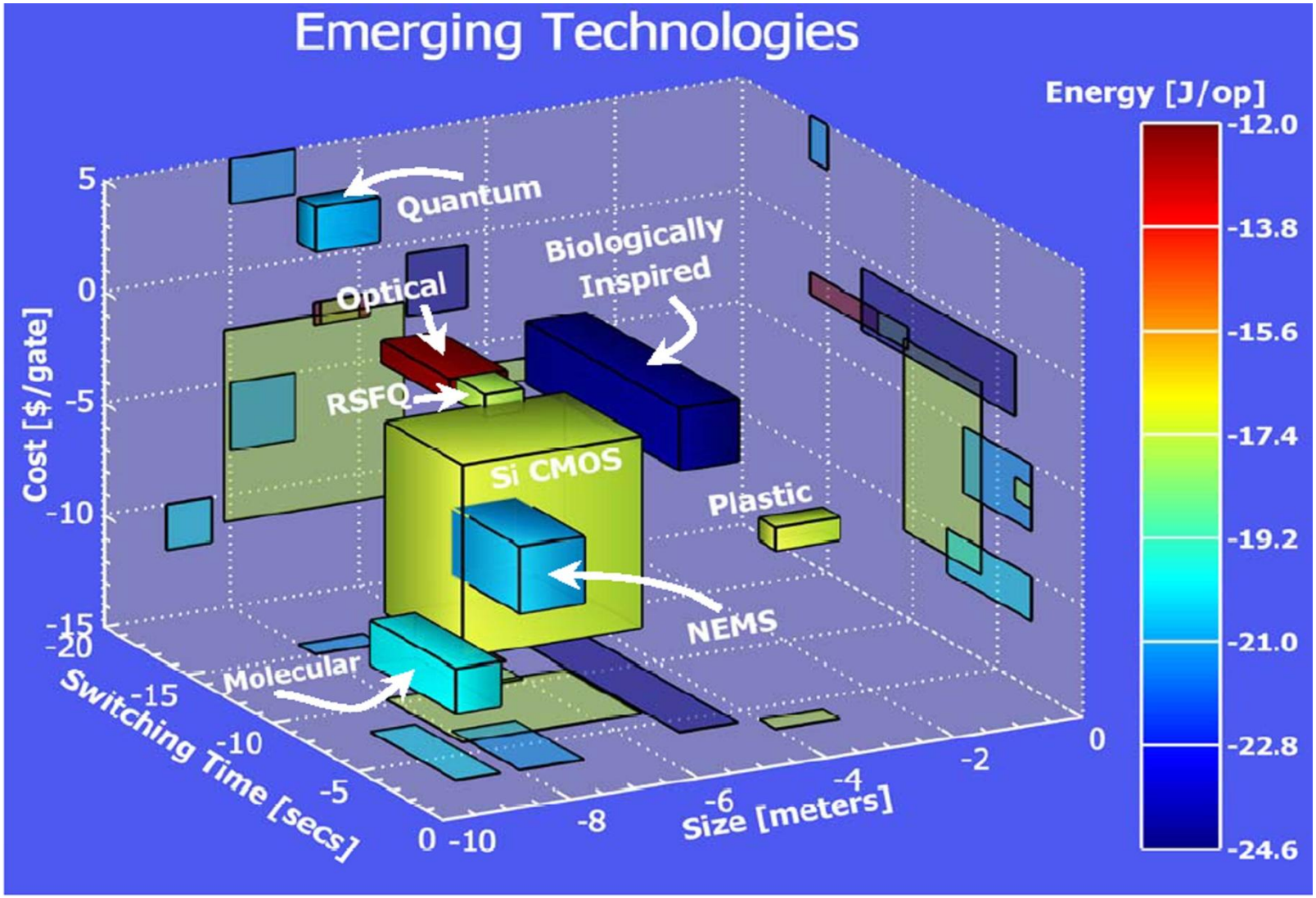
В.П. Попов

Прогнозируемые и достигнутые параметры логических элементов

Device								
			FET Extension					
		FET [A]	*1D structures*	*Channel replacement*	*SET*	*Molecular*	*Ferromagnetic logic*	*Spin transistor*
Typical example devices		Si CMOS	CNT FET NW FET NW hetero-structures Nanoribbon transistors with graphene	III-V compound semiconductor and Ge channel replacement	SET	Crossbar latch Molecular transistor Molecular QCA	Moving domain wall M: QCA	Spin Gain transistor Spin FET Spin Torque Transistor
Cell Size (spatial pitch) [B]	Projected	100 nm	100 nm [D]	300 nm [I]	40 nm [O]	10 nm [U]	140 nm [Y]	100 nm [C]
	Demonstrated	590 nm	~1.5 μm [E]	1700 nm [J]	~200 nm [K, L]	~2 μm [V]	250 nm [Z, AA]	100 μm [AB]
Density (device/cm^2)	Projected	1E10	4.5E9	6.1E9	6E10	1E12	5E9	4.5E9
	Demonstrated	2.8E8	4E7	3.5E7	~2E9	2E7	1.6E9	1E4
Switch Speed	Projected	12 THz	6.3 THz [F]	>1 THz	10 THz [Q]	1 THz [W]	1 GHz [Y]	40 GHz [AC]
	Demonstrated	1.5 THz	200 MHz [G]	>300 GHz	2 THz [R]	100 Hz [V]	30 Hz [Z, AA]	Not known
Circuit Speed	Projected	61 GHz	61 GHz [C]	61 GHz [C]	1 GHz [O]	1 GHz [U]	10 MHz [Y]	Not known
	Demonstrated	5.6 GHz	220 Hz [H]	Data not available	1 MHz [P]	100 Hz [V]	30 Hz [Z]	Not known
Switching Energy, J	Projected	3E-18	3E-18	3.00E-18	1×10^{-18} [O] [$>1.5\times10^{-17}$] [S]	5E-17 [X]	~1E-17 [Z]	3E-18
	Demonstrated	1E-16	1E-11 [H]	1E-16 [J]	8×10^{-17} [T] [$>1.3\times10^{-14}$] [S]	3E-7 [V]	6E-18 [AA]	Not known
Binary Throughput, GBit/ns/cm^2	Projected	238	238	61	10	1000	5E-2	Not known
	Demonstrated	1.6	1E-8	Data not available	2E-4	2E-9	5E-8	Not known
Operational Temperature		RT	RT	RT	RT [M, N]	RT	RT	RT
Materials System		Si	CNT, Si, Ge, III-V, In_2O_3, ZnO, TiO_2, SiC,	InGaAs, InAs, InSb	III-V, Si, Ge,	Organic molecules	Ferromagnetic alloys	Si, III-V, complex metals oxides
Research Activity [AD]			379	62	91	244	32	122

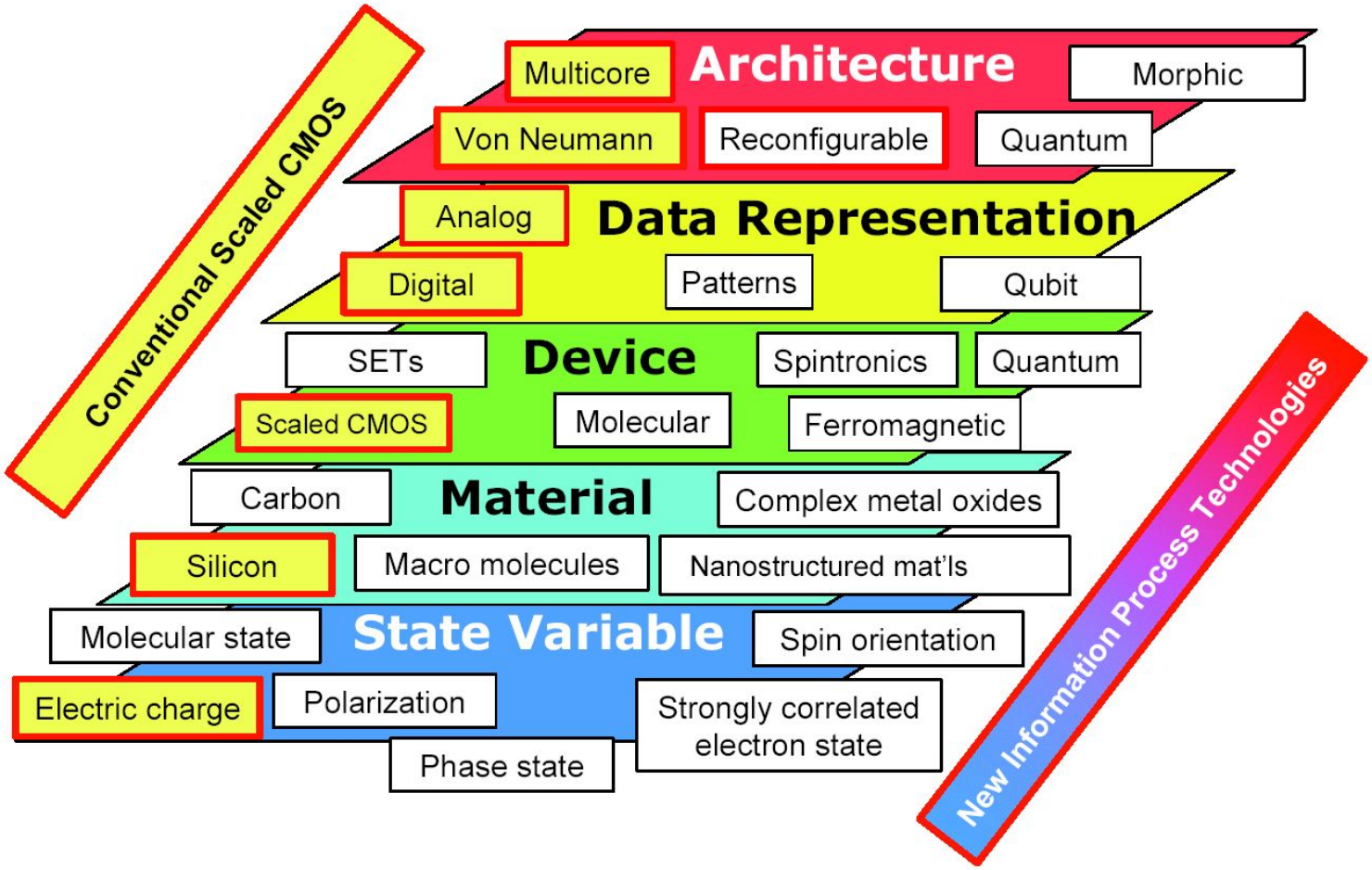
**The International Technology Roadmap for Semiconductors*, edn. 2007

Технико-экономические параметры элементных базисов



The International Technology Roadmap for Semiconductors, edn. 2003

Развивающиеся и поисковые информационные технологии



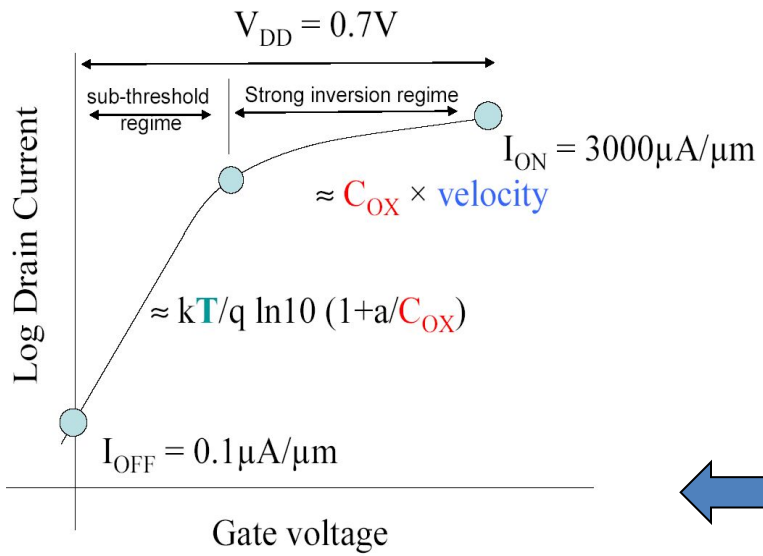
The International Technology Roadmap for Semiconductors, edn. 2007

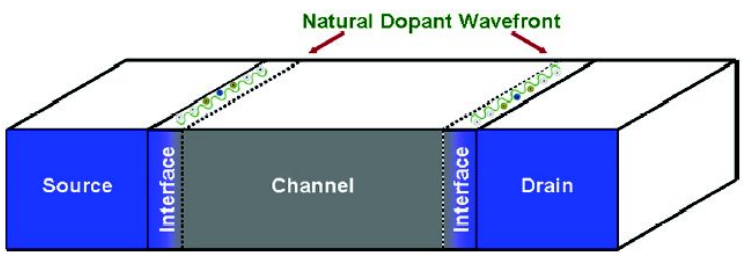
Принцип электростатического подобия и закон Мура

$P_{dyn} = n \cdot I_{on} \cdot V_{DD} \rightarrow k^{-2} \cdot k \cdot k = const$ $\quad k \sim 0.7$

$F_{dyn} = I_{on} / (C_{ox} \cdot W \cdot L \cdot V_{DD}) \rightarrow k / (k^{-1} \cdot k \cdot k \cdot k) = k^{-1}$

Текущее масштабирование по мощности и частоте для схем на классических КМОП транзисторах





** L_g = 5 nm n-MOSFET*

Lch = 6 ± 3 nm из-за флуктуаций $n^+_{S,D}$

<u>*Ограничения нанотранзисторов:*</u>

Предел масштабирования по туннельному току затвора I_G достигнут при 90 нм норме *GOT = 1.5 nm*

Для 45 nm – high-k диэлектрики *GOT = 1.0 nm* Для 14 nm – GOT = 0.5 nm (SiO_2)

При 14 нм проектной норме (2015 г.)* – баллистический режим (L< λ) , но туннелирование S-D

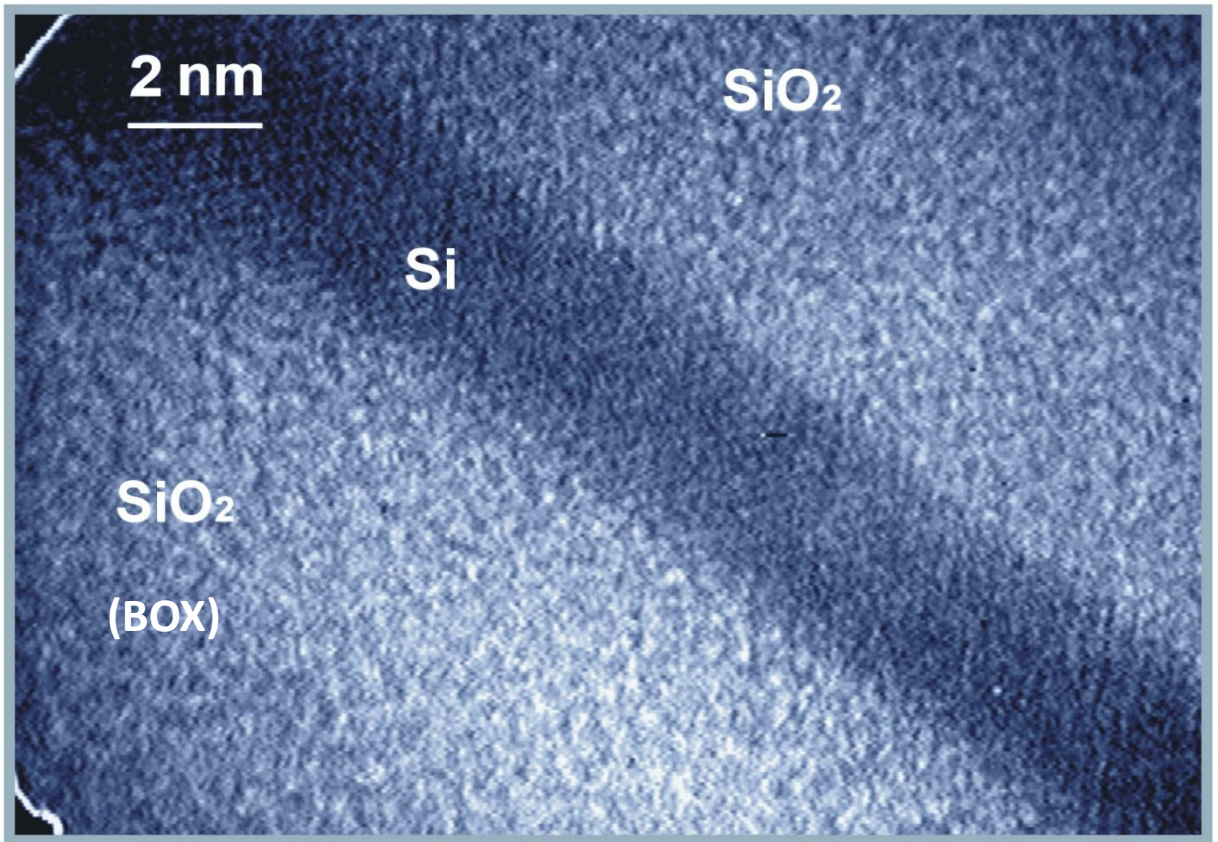
При L=3 нм (10 нм норма 2020 г.) - изменения зонной структуры (скорости, ёмкости)

- Снижение температуры
- Уменьшение ёмкости оксида
- Увеличение скорости

.....или инженерия канала?

**The International Technology Roadmap for Semiconductors*, edn. 2006

Silicon-on-Isolator (SOI) ultra-thin structure



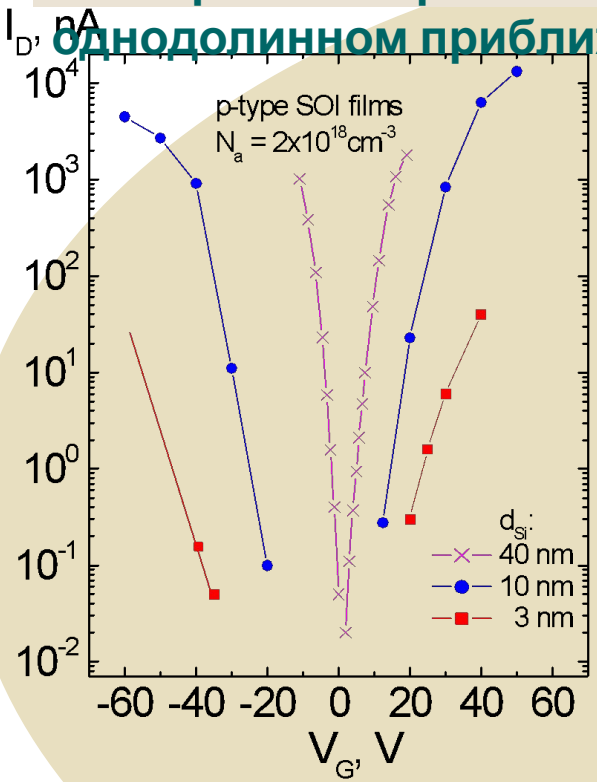
Electron microphotography with atomic resolution of cross-section of mono-crystalline ultra-thin cut-off 3 nm silicon layer between upper oxide and buried dielectric of SOI-structure

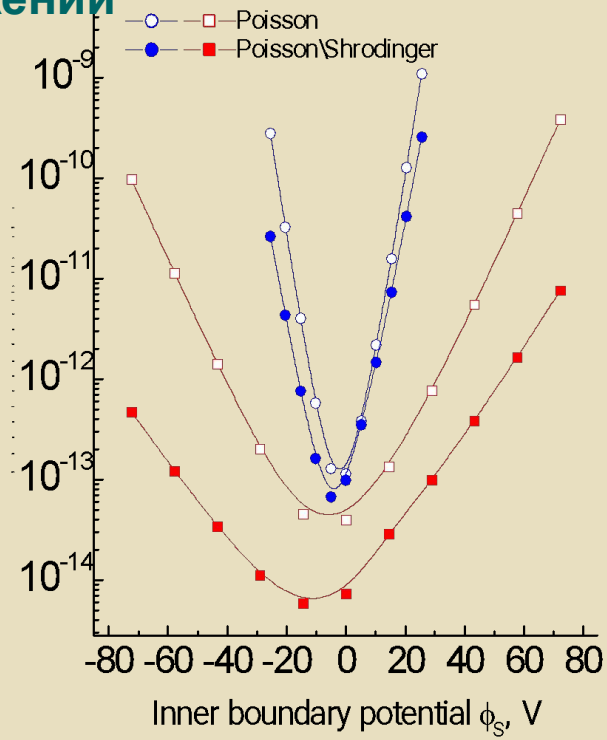
World record presented in 1999 at E-MRS Meeting

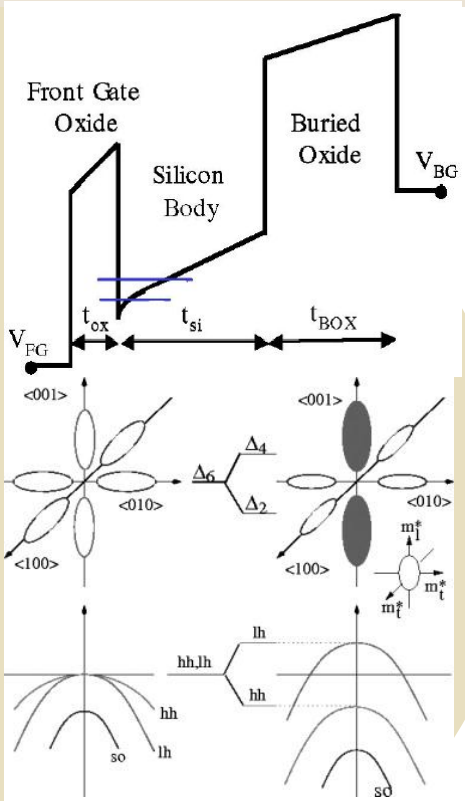
V.P. Popov, I.V. Antonova, V.F. Stas et al., J. Mater. Sci. Eng. B, 73, 82 (2000)

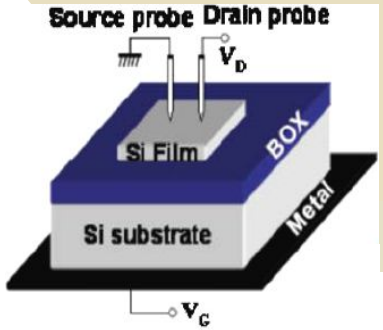
Проводимость 3 нм пленок Si в КНИ: измерения ВАХ точечно-контактного псевдо МОП-транзистора и расчет DOS в ОДП

Эксперимент и расчет плотности состояний (DOS) плёнки Si в однодолинном приближении









$$E_{Л} = \frac{h^2\pi^2}{2m^*_{Л}d^2_{Si}} = 23{,}5\text{мэВ} \qquad E_{l} = \frac{h^2\pi^2}{2m_{l}d^2_{Si}} = 19{,}8\text{мэВ}$$

$$E_i^{L,T} = \left(\frac{\hbar^2}{2\,m_{L,T}}\right)\left(\frac{3\pi\, q\, E^{L,T}_{eff\ i}}{2}\cdot \eta_i\right)^{2/3}$$

Квантовые поправки в проводимость 3 нм канала – 1-2 порядка

V.P. Popov, I.V. Antonova, V.F. Stas et al., J. Mater. Sci. Eng. B, 73, 82 (2000)

Проводимость 3 нм пленок Si в КНИ: измерения ВАХ точечно-контактного псевдо МОП-транзистора и расчет DOS в ОДП

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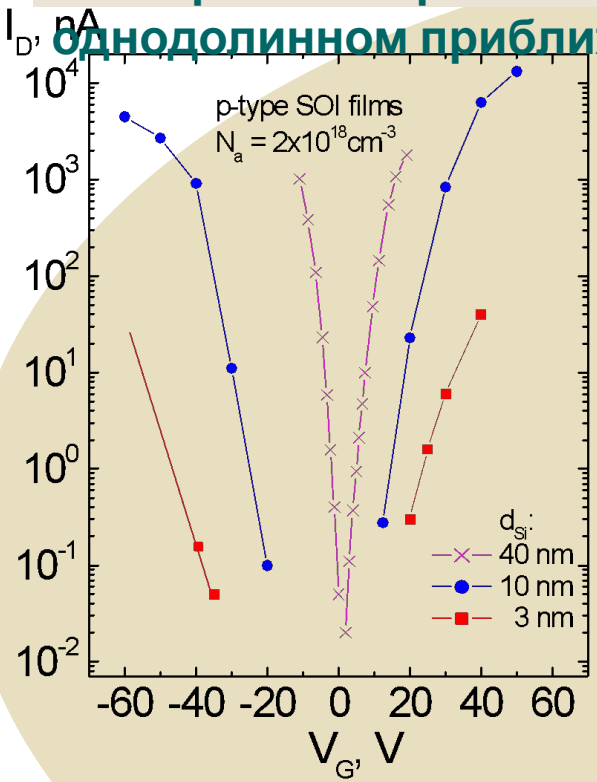

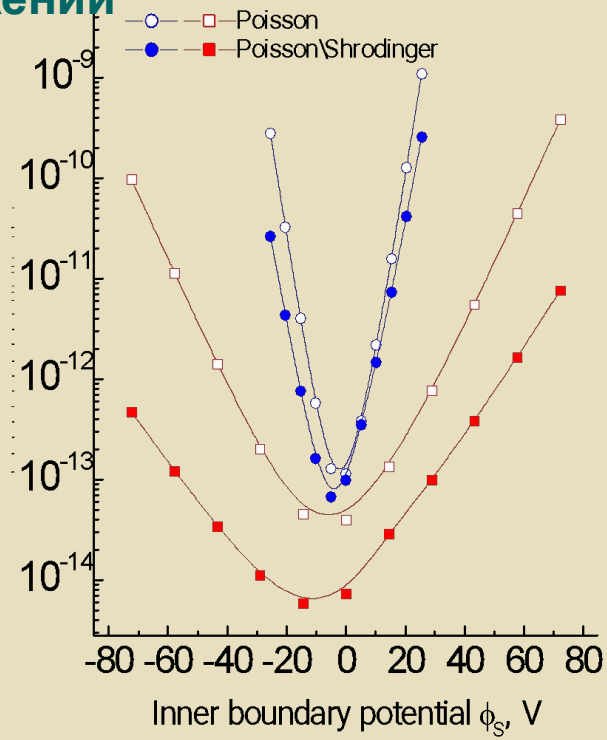

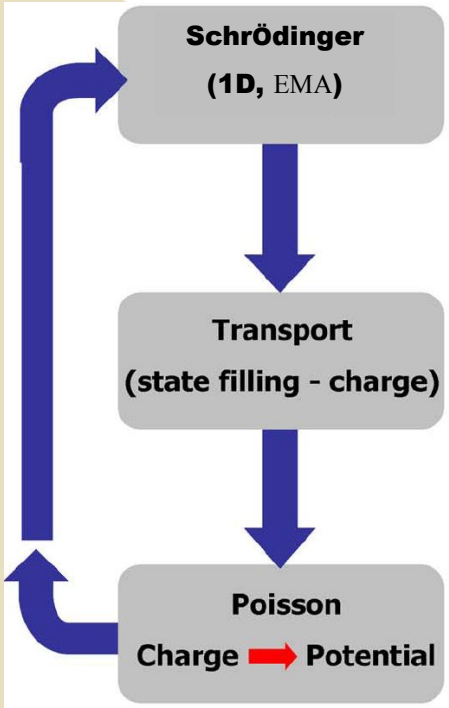

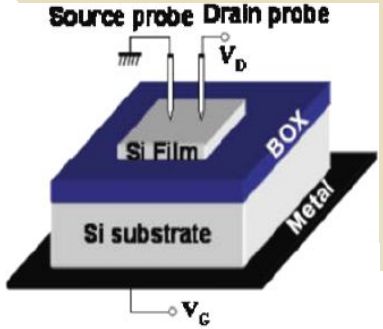

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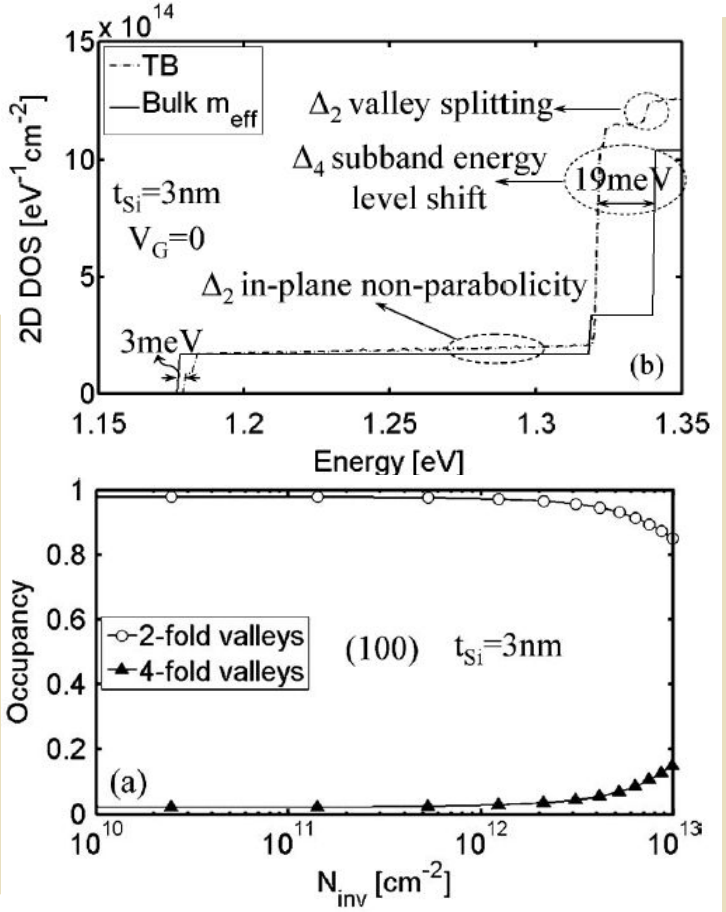
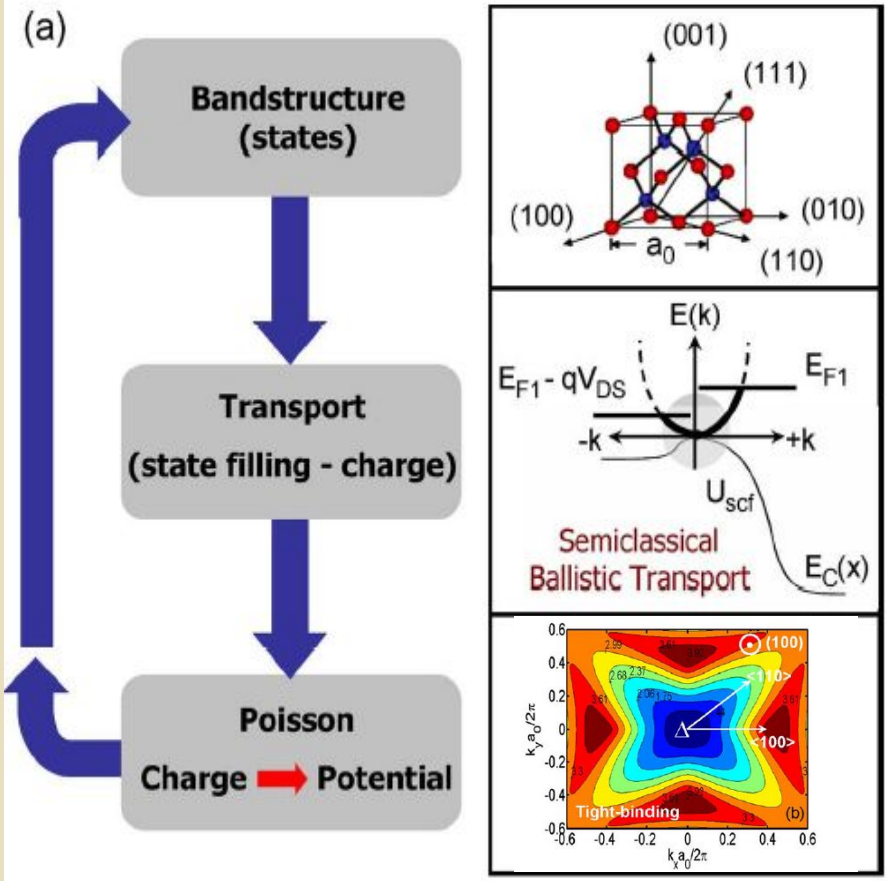
V.P. Popov, I.V. Antonova, V.F. Stas et al., J. Mater. Sci. Eng. B, 73, 82 (2000)

Проводимость 3 нм пленок Si в КНИ: расчет DOS в EMA и TB





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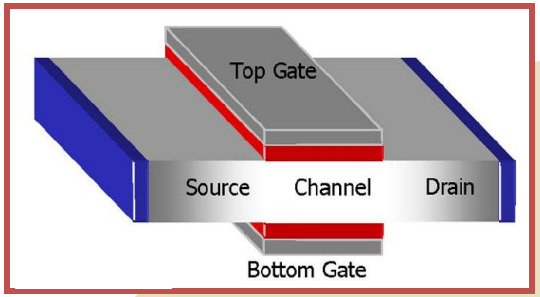
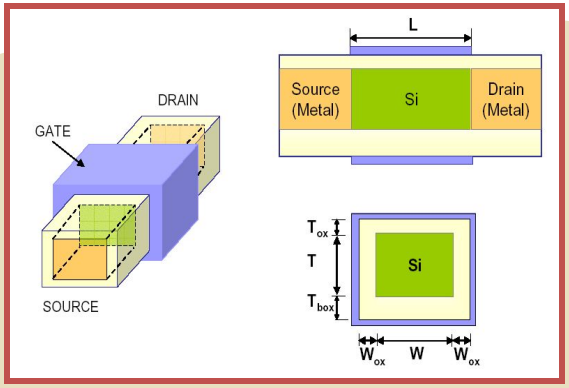
www.nanohub.org

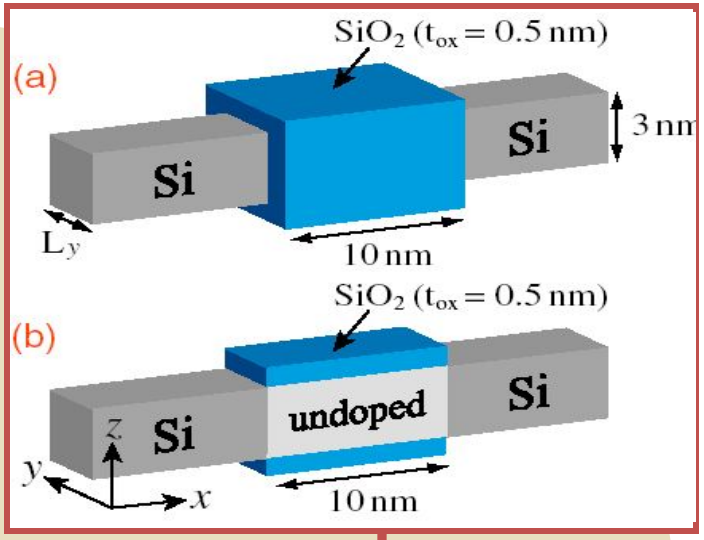
Квантовые поправки определяются зонной структурой и зарядом

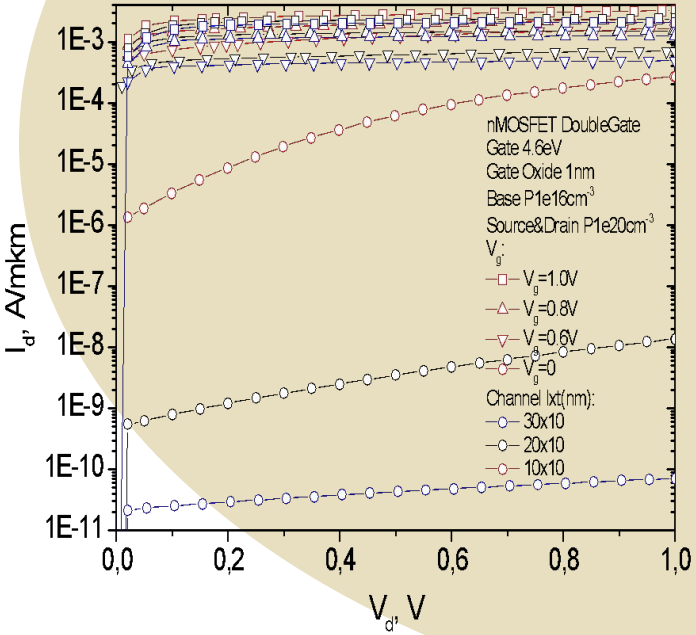
M. Lundstrom et al., IEEE TRANS. ON ELECTRON DEV., 55, 866(2008)

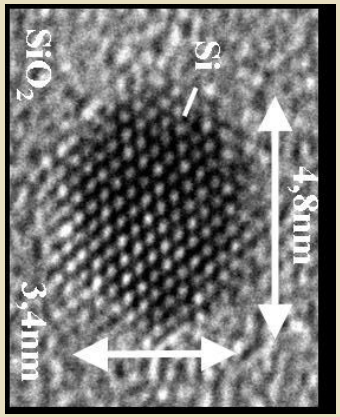
Переключение тока (on-off) в двухзатворном (DG) и нанопроволочном (SNW) транзисторах

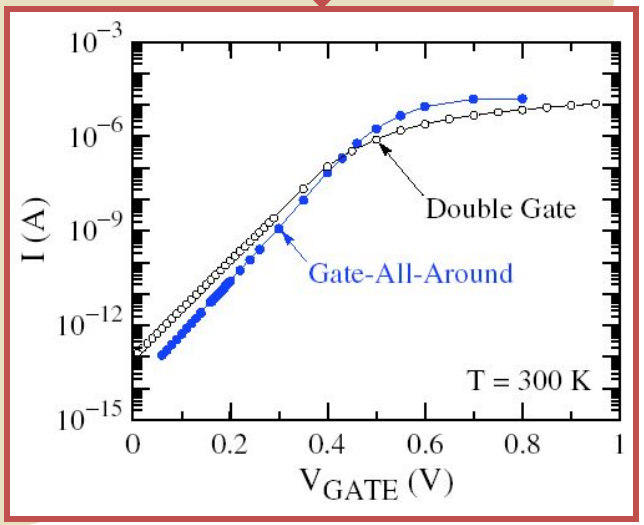












O.V. Naumova, M.A. Ilnitsky, L.N. Safronov, V.P. Popov. Semicond., v. 41, p.103-109, 2007

www.nanohub.org M. Lundstrom et al. IEEE Trans. on Elect. Dev., 55, 1286, 2008

*M.Shin M.Shin, IEEE Transactions On Nanotechnology **6**, 230 (200*

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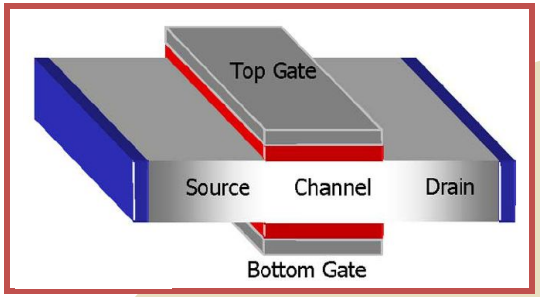

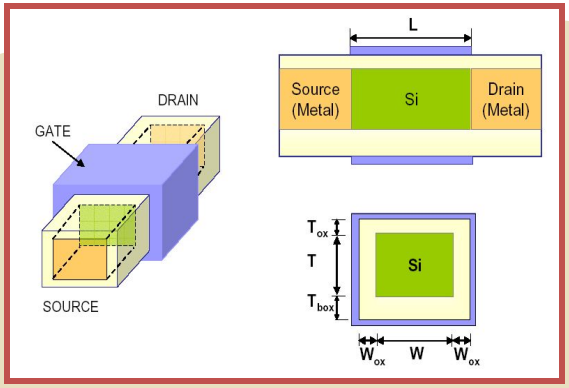

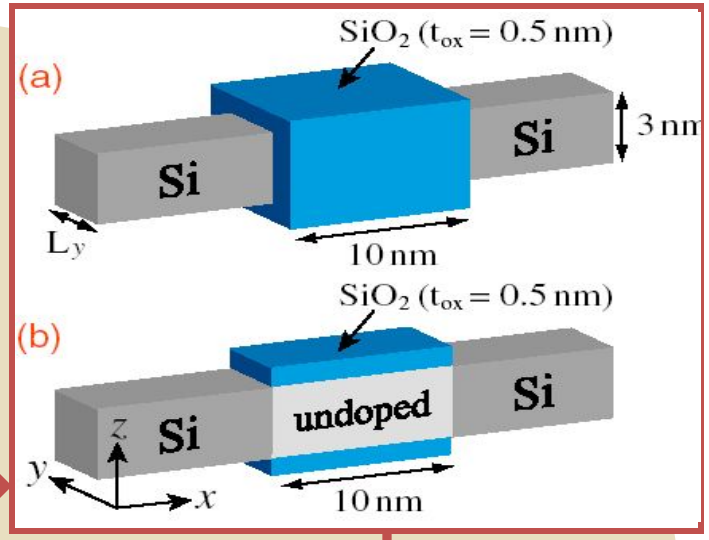

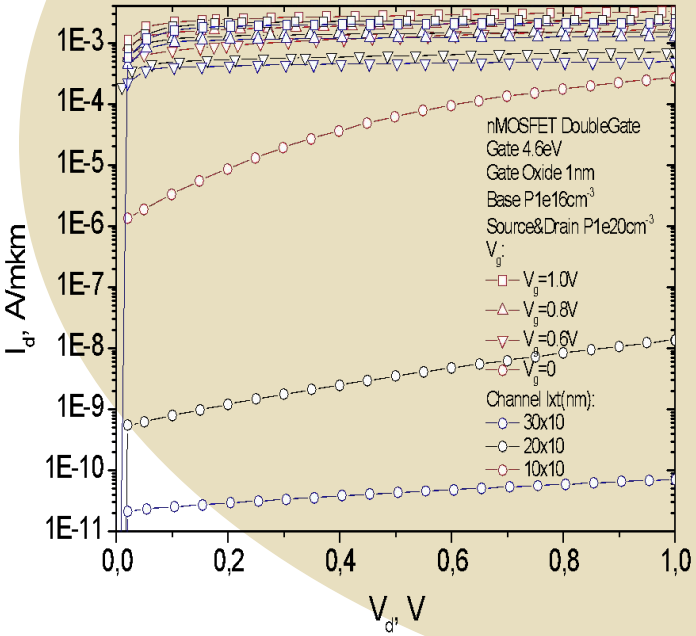

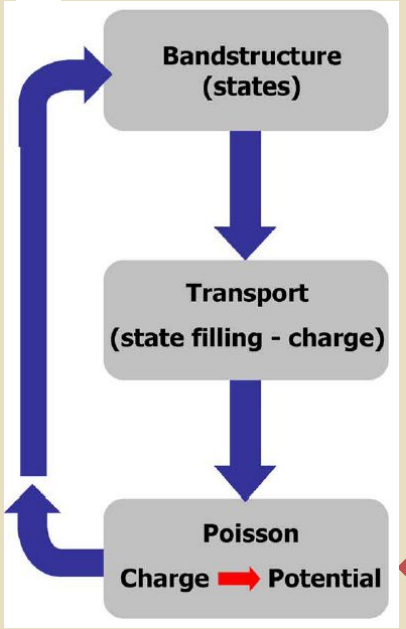

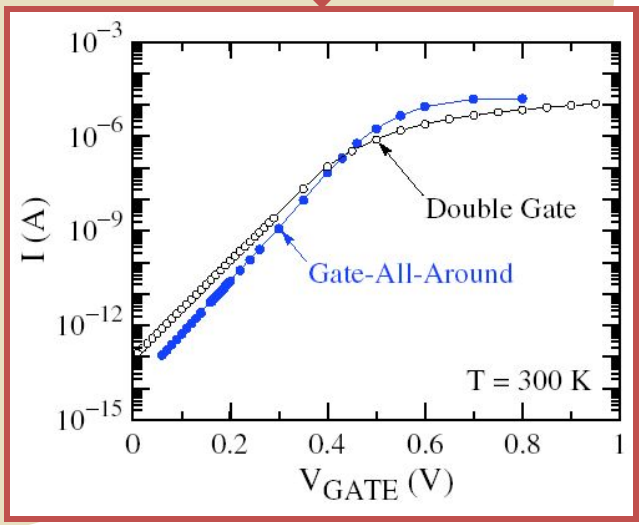

O.V. Naumova, M.A. Ilnitsky, L.N. Safronov, V.P. Popov. Semicond., v. 41, p.103-109, 2007

www.nanohub.org M. Lundstrom et al. IEEE Trans. on Elect. Dev., 55, 1286, 2008

M.Shin M.Shin, IEEE Transactions On Nanotechnology 6, 230 (200

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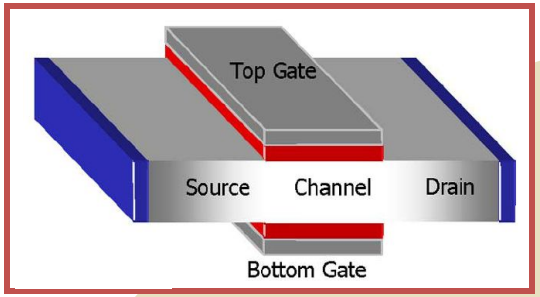
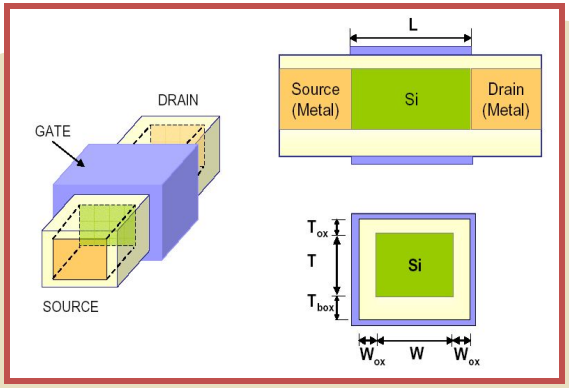
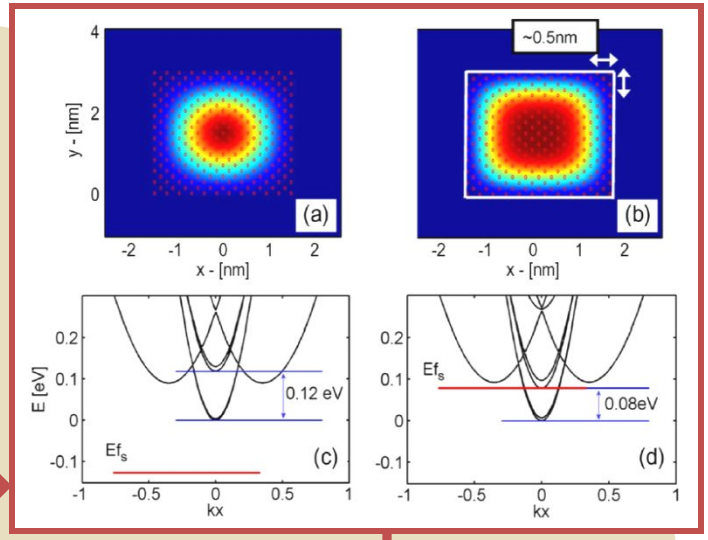
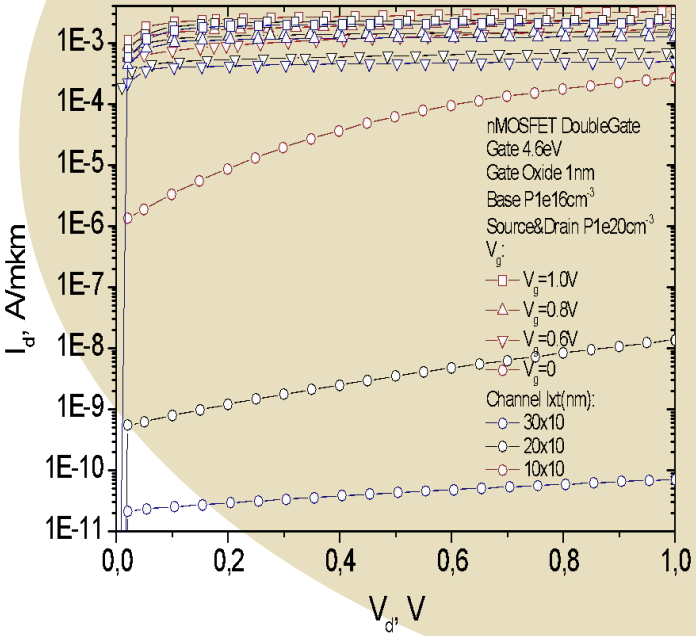
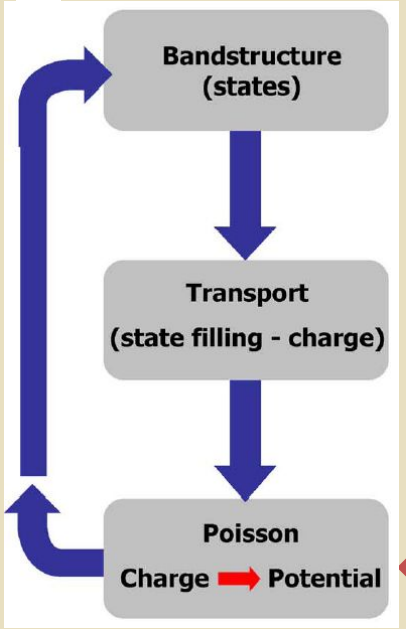
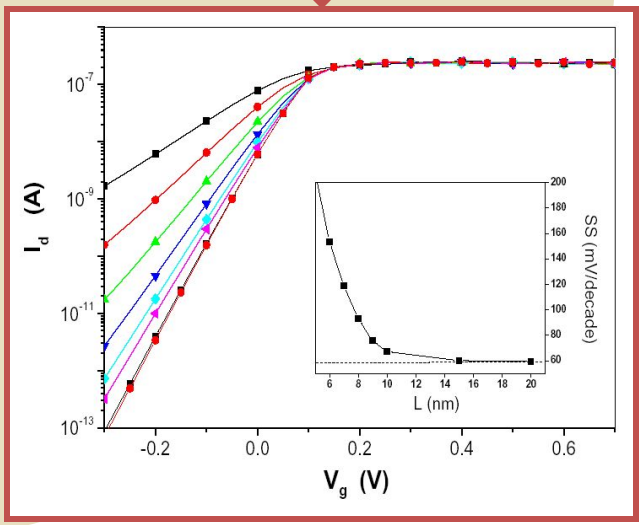










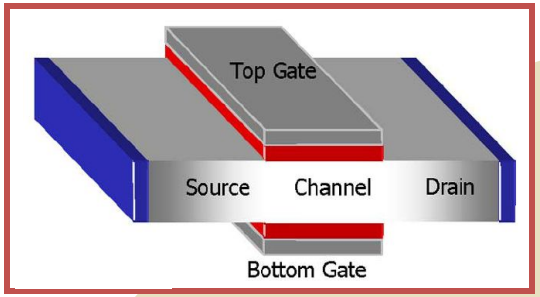


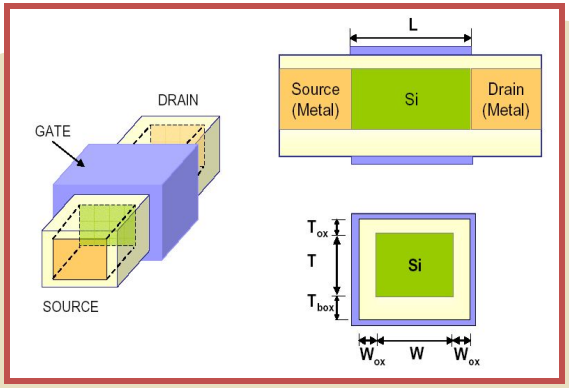
O.V. Naumova, M.A. Ilnitsky, L.N. Safronov, V.P. Popov. Semicond., v. 41, p.103-109, 2007

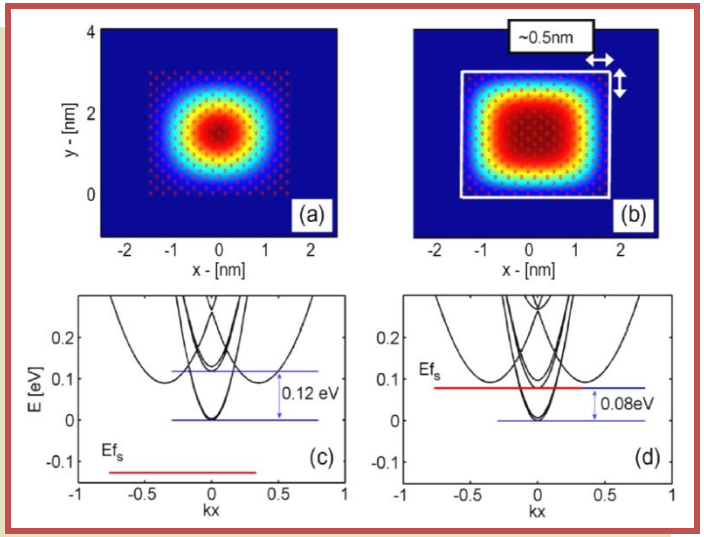
www.nanohub.org M. Lundstrom et al. IEEE Trans. on Elect. Dev., 55, 1286, 2008

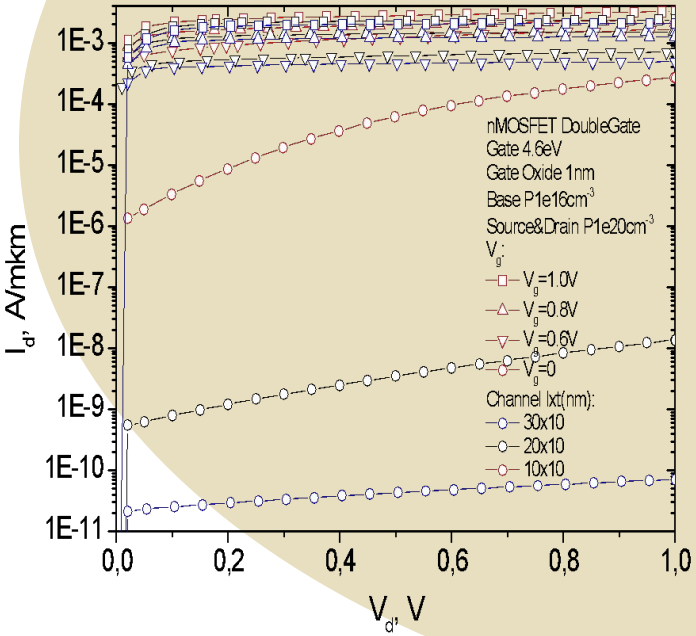
M.Shin M.Shin, IEEE Transactions On Nanotechnology 6, 230 (200

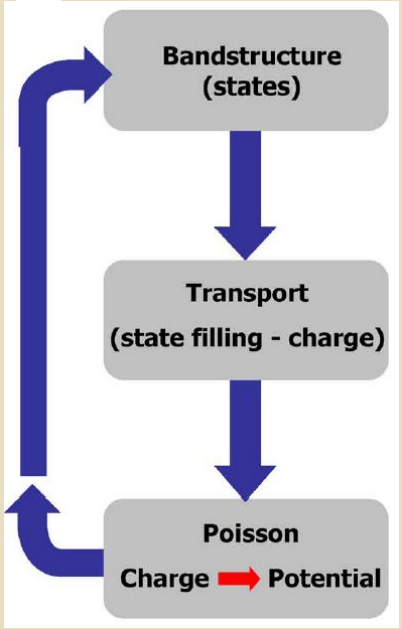
Переключение тока (on-off) в двухзатворном (DG) и нанопроволочном (SNW) транзисторах

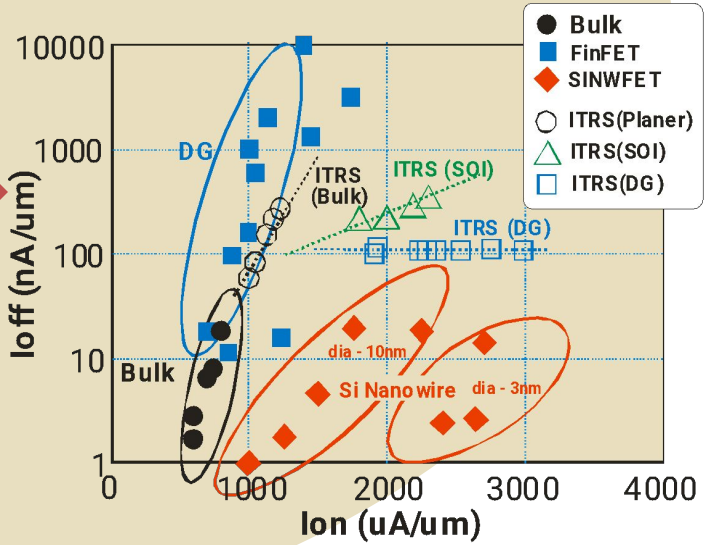












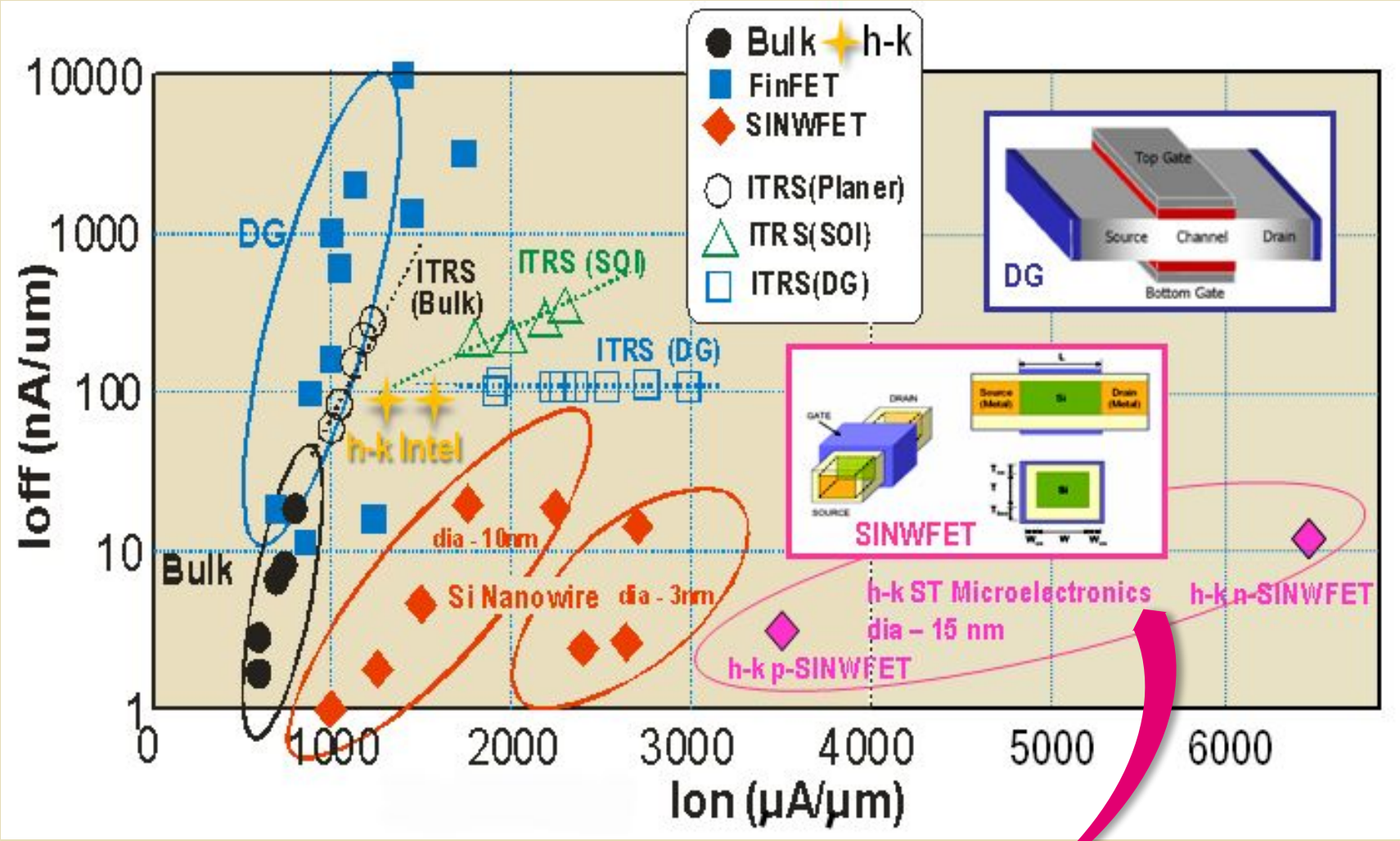
Ion / Ioff разных типов нанотранзисторов

O.V. Naumova, M.A. Ilnitsky, L.N. Safronov, V.P. Popov. Semicond., v. 41, p.103-109, 2007

www.nanohub.org *M. Lundstrom et al. IEEE Trans. on Elect. Dev., 55, 1286, 2008*

H. Iwai 4th Int. Symp. on Adv. Gate Stack Technol., 2007

Двухзатворные (DG) и нанопроволочые (SINW) транзисторы для СБИС



IEDM 2008: high-k SiNWT with 10 nm

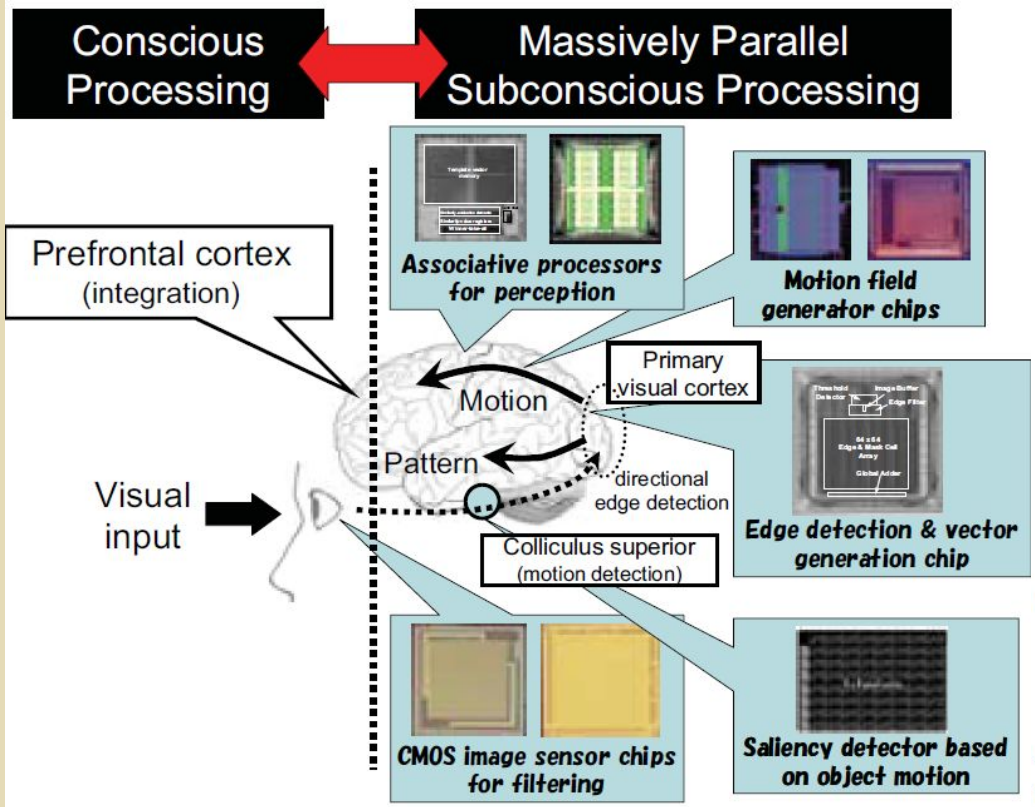
Intel high-k 32 nm technology

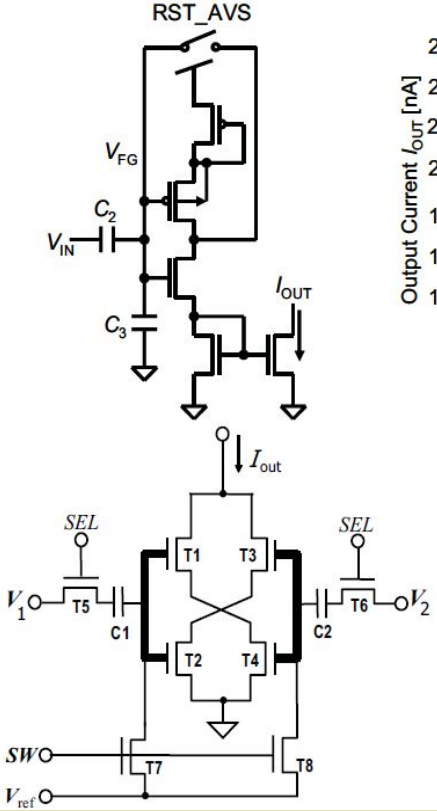
H. Iwai 4th Int. Symp. on Adv. Gate Stack Technol., 2007

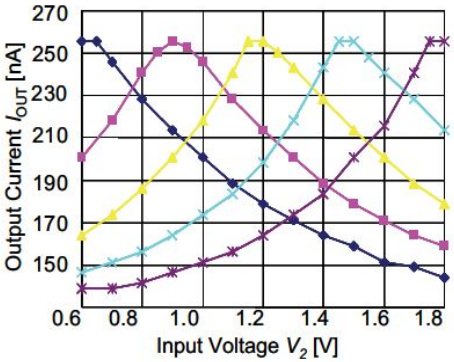
S. Deleonibus et al. 31.2 IEDM 2008

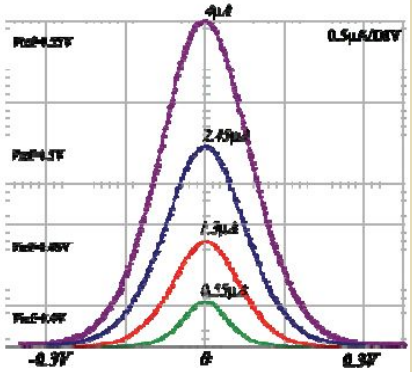
Sanjay Natarajan et al. IEDM 2008

КМОП СБИС чип эмуляции процессов опознавания, обучения и принятия решений







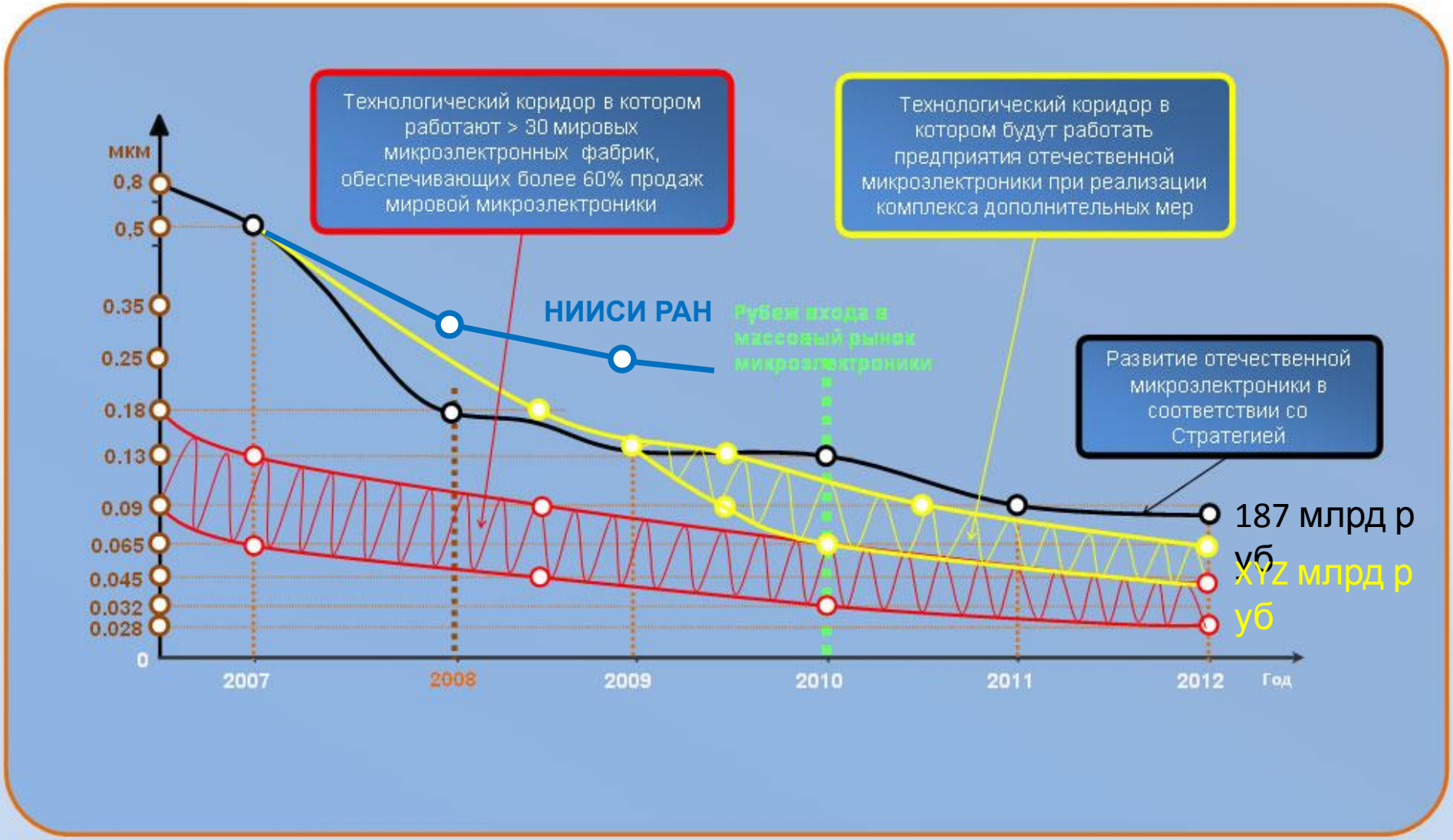


Архитектура кремниевого чипа с ~10 млрд. КМОП транзисторов, эмулирующих мозг (Тадаши Шибата)

Резонансные характеристики логики для ассоциативных «голосующих» процессоров на КМОП и NМОП нанотранзисторах

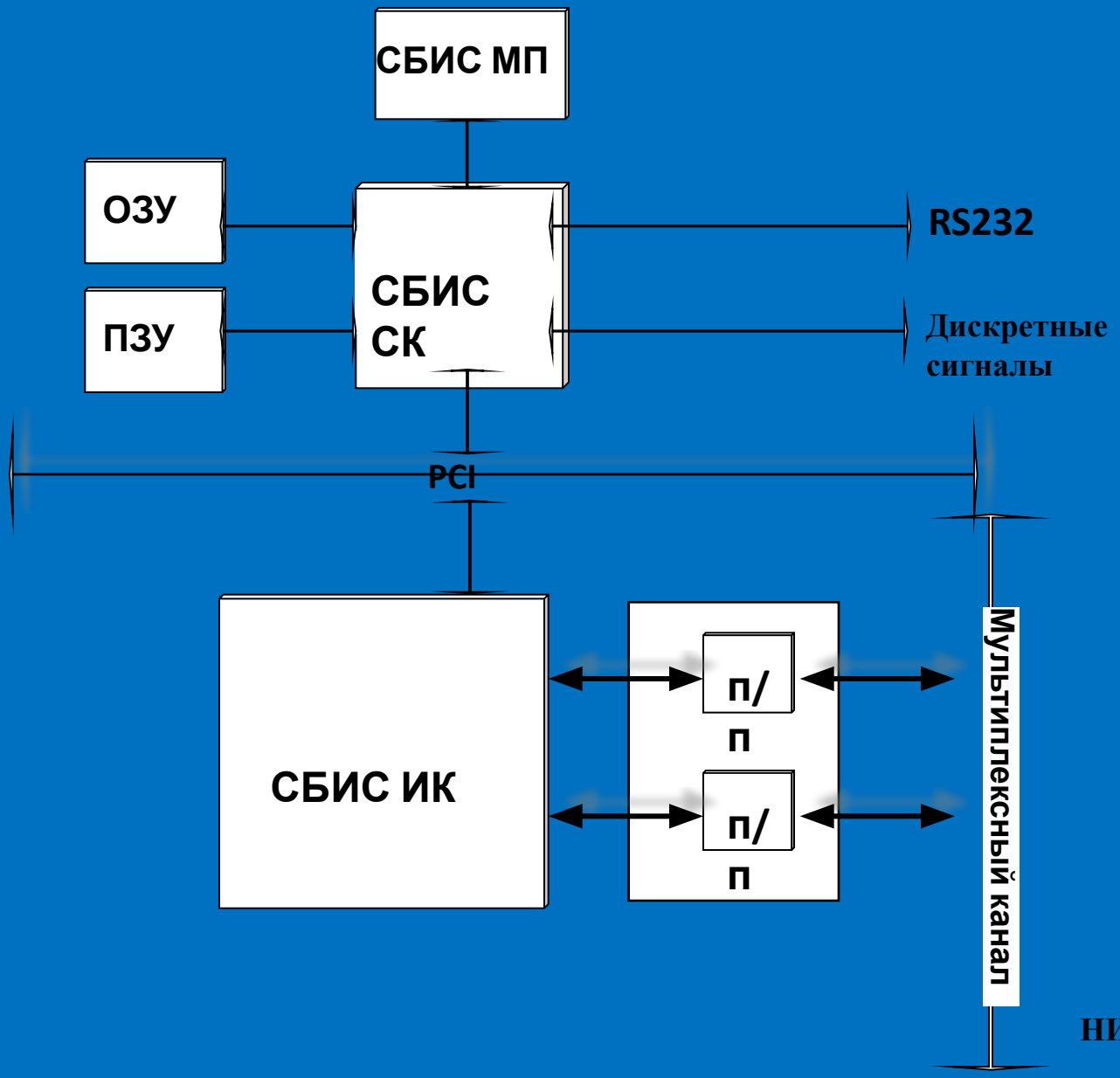
T. Shibata et al., *Proc. 10th Int. Conf. Ultimate Integration of Silicon (ULIS), 233, March, 2009.*

Техпроцессы системообразующей ЭКБ микроэлектроники



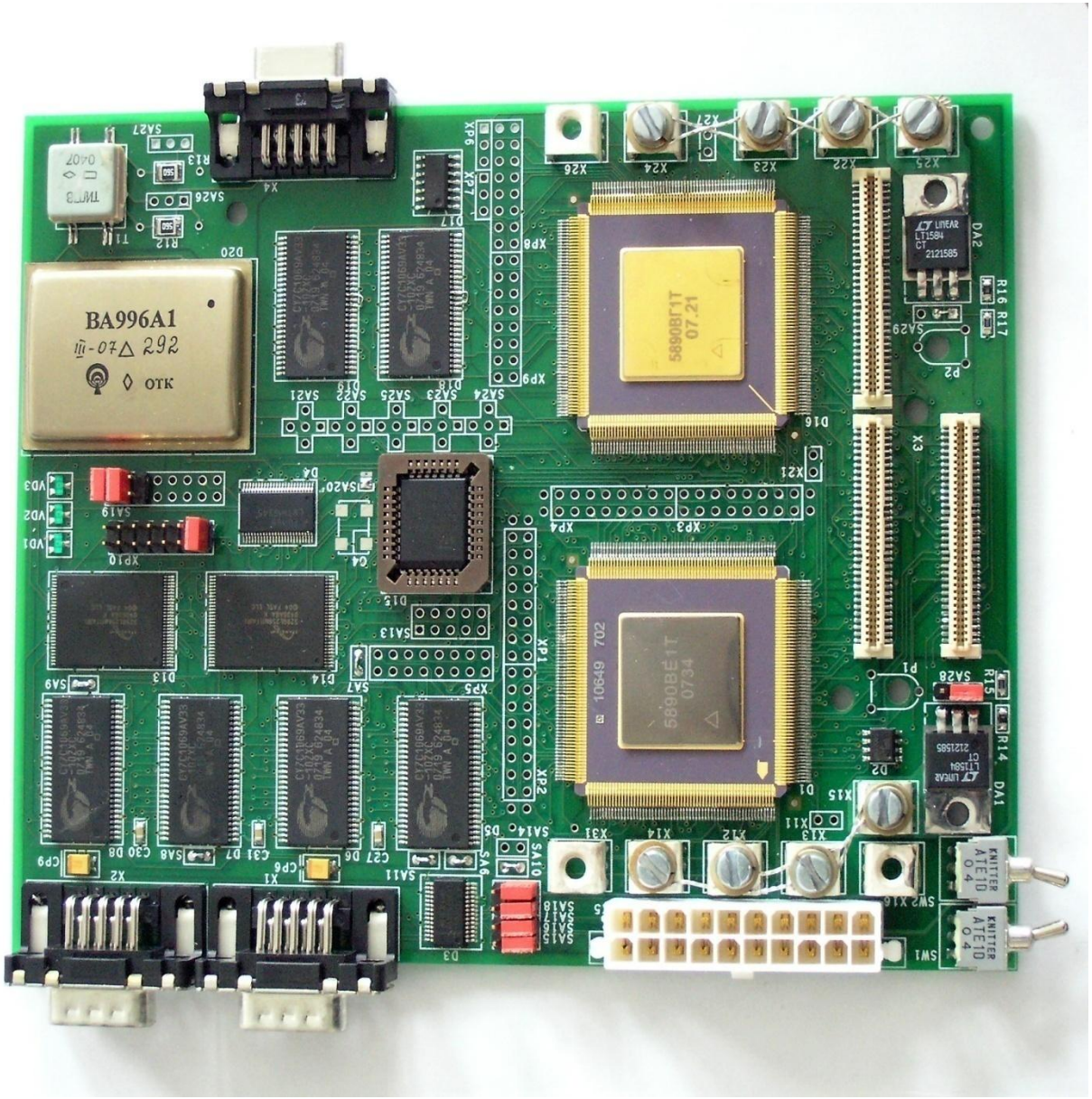
*Совещание по развитию электронной промышленности РФ, сент. 2008

Структура управляющей ЭВМ с 32-разрядным RISC микропроцессором КОМДИВ32-С



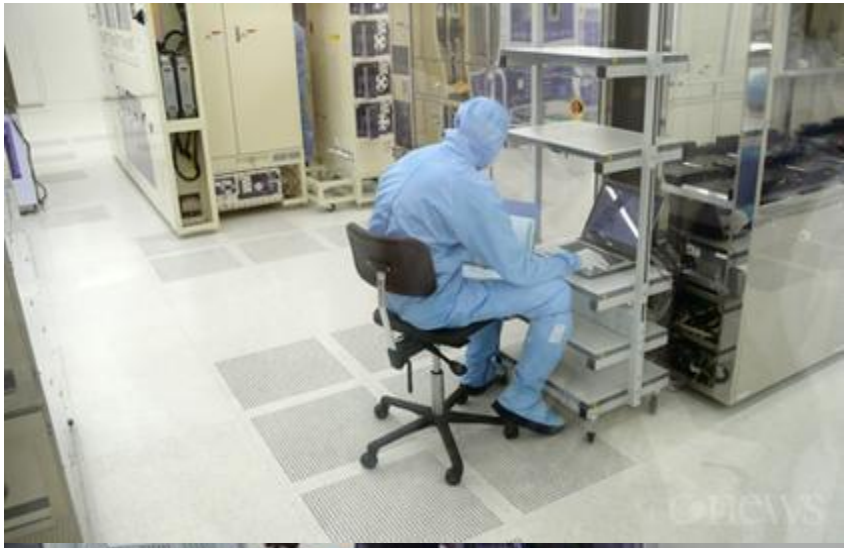
НИИСИ РАН, 2008

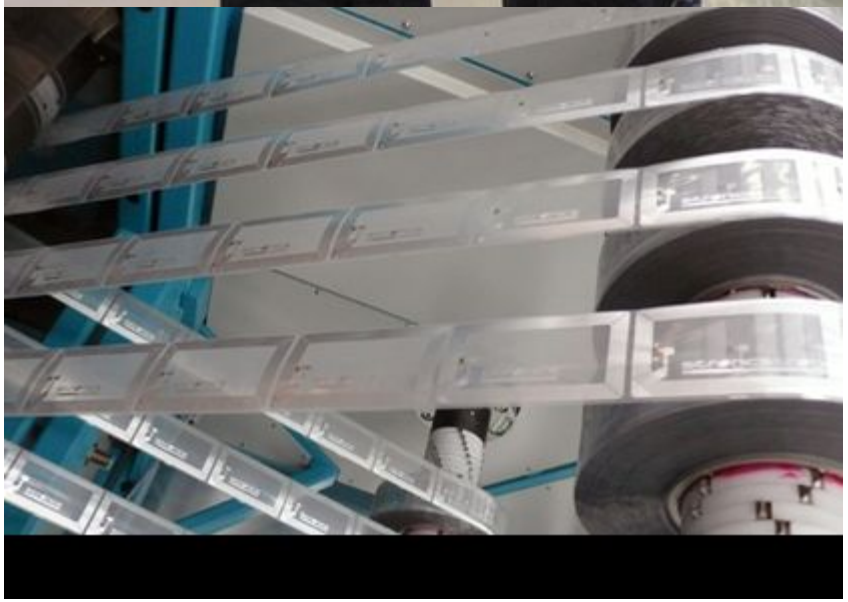
Плата управляющей ЭВМ с 32-разрядным RISC микропроцессором КОМДИВ32-С



НИИСИ РАН, 2008

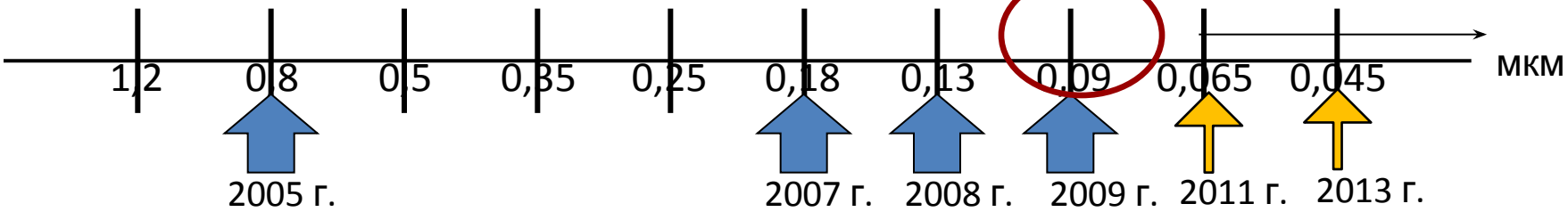
0.18 мкм технология ST Microelectronics 2007г.

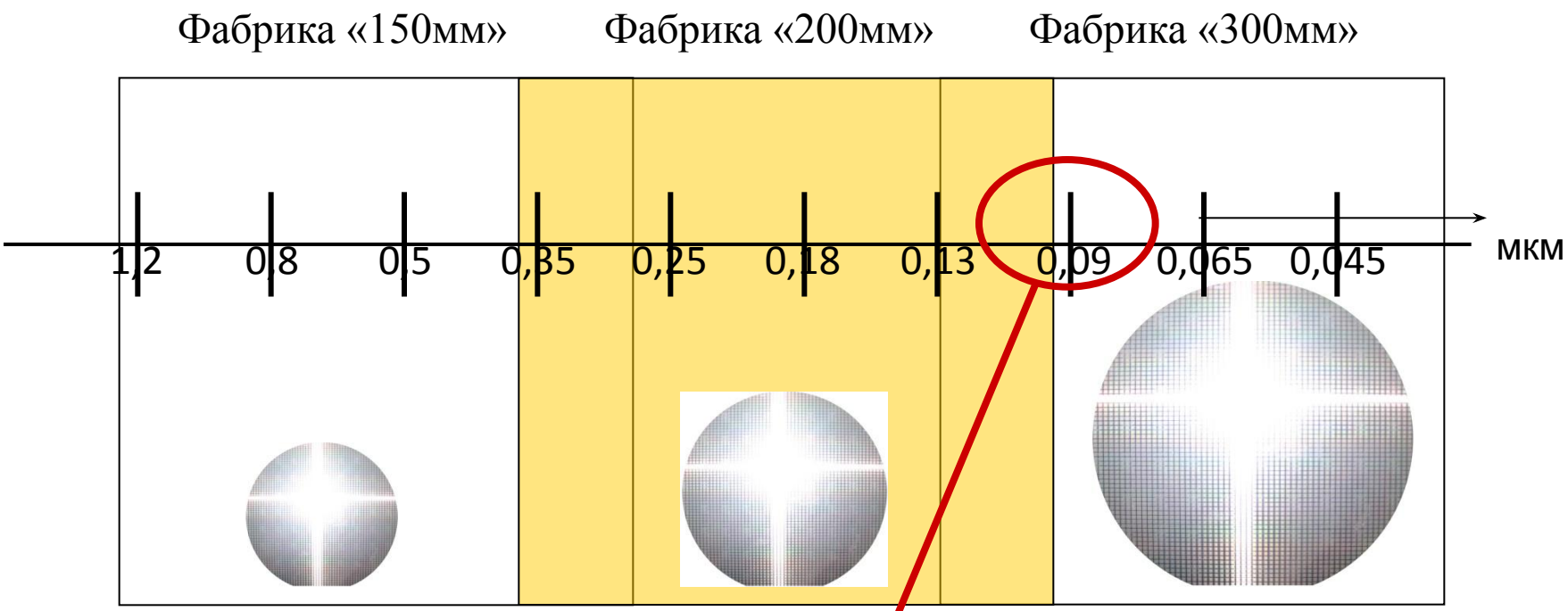




Планы технологического развития «НИИМЭ и Микрон»

Модернизация 200мм фабрики в 2011г. с Роснано





Строительство новой 300мм фабрики
для уже существующей на 200мм технологии

Результаты и перспективы развития КМОП технологии

- - Имеющийся научно-технический задел по кремниевой КМОП технологии позволяет прогнозировать масштабированное уменьшение размеров от 45 нм до 4-5 нм в течение ближайших 20-25 лет. Дальнейший прогресс бинарной (цифровой) логики будет основан не на принципах переноса заряда или спина.

- - Существующий сегодня уровень интеграции в КМОП СБИС достаточен для формирования многопроцессорных параллельных систем, в том числе систем ассоциативной логики.

- - Одновременная разработка новых материалов (графена, п/п наноструктур, квантовых точек) и новой архитектуры микропроцессоров являются необходимым условием создания искусственного интеллекта, не уступающего по уровню человеку.

- - Отставание России от мировых лидеров в развитии подобных систем

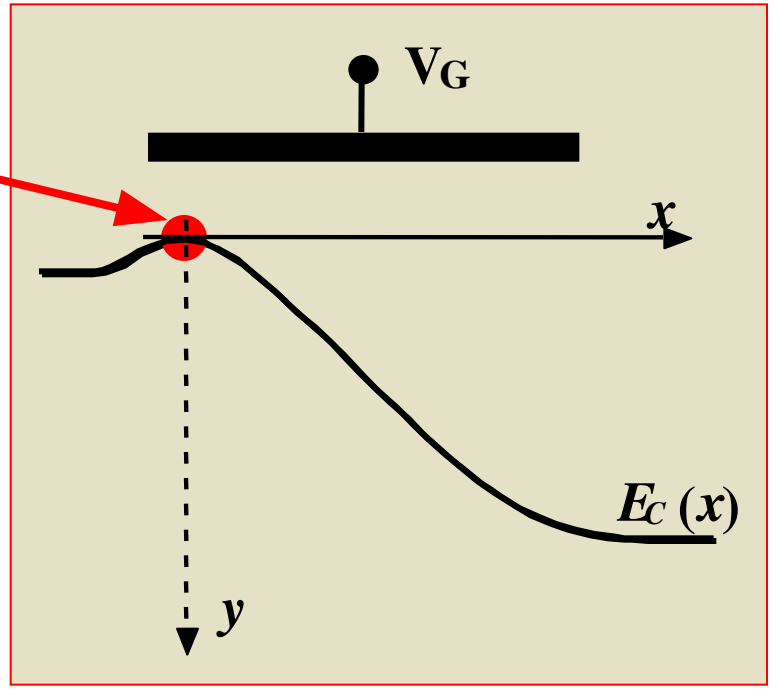
Проблема плотности тока при размерном квантовании

ток, зависящий от пропускания.....

квази-равновесие

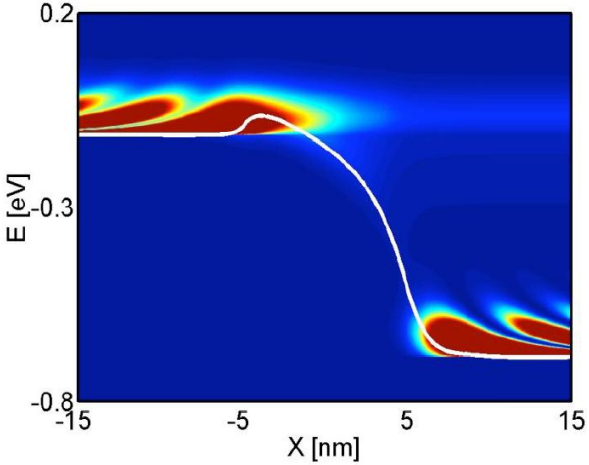
$n_S(V_{GS}) = C_{eff}(V_{GS} - V_T)$

Аппроксимация плавного канала + DIBL



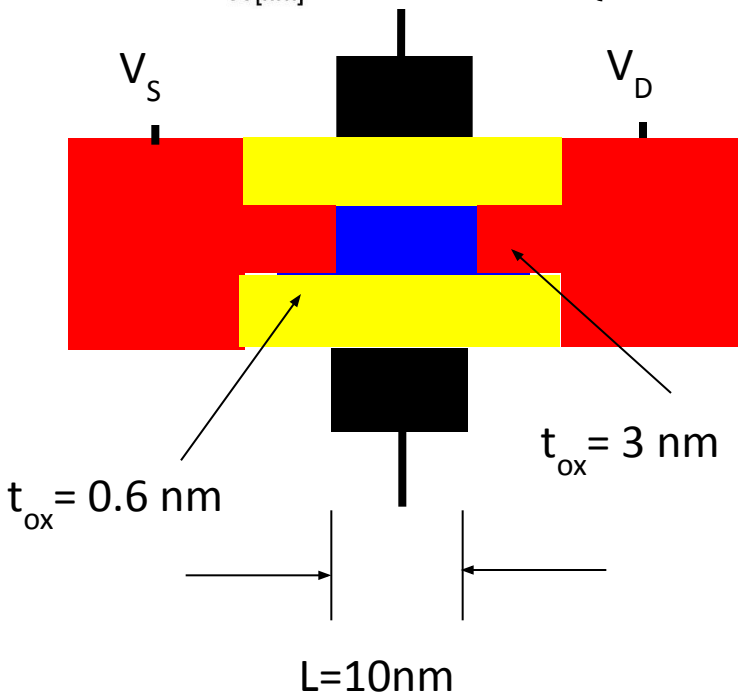
$$I_{DS} = W C_{ox} \upsilon_T (V_{GS} - V_T) \left[\frac{1 - e^{-qV_{DS}/k_B T_L}}{1 + e^{-qV_{DS}/k_B T_L}} \right] \qquad \upsilon_T = \sqrt{\frac{2 k_B T_L}{\pi m^*}}$$

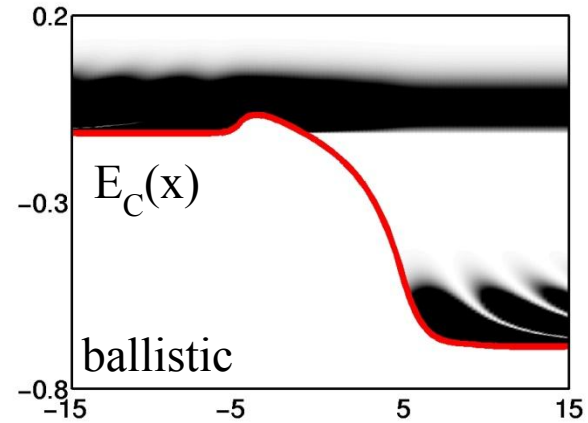
(Статистика Больцмана и одна подзона)

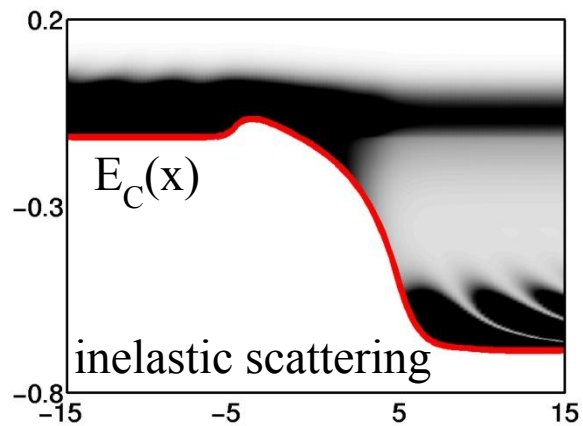


I-V characteristics of nano-MOSFETs

effective mass Hamiltonian

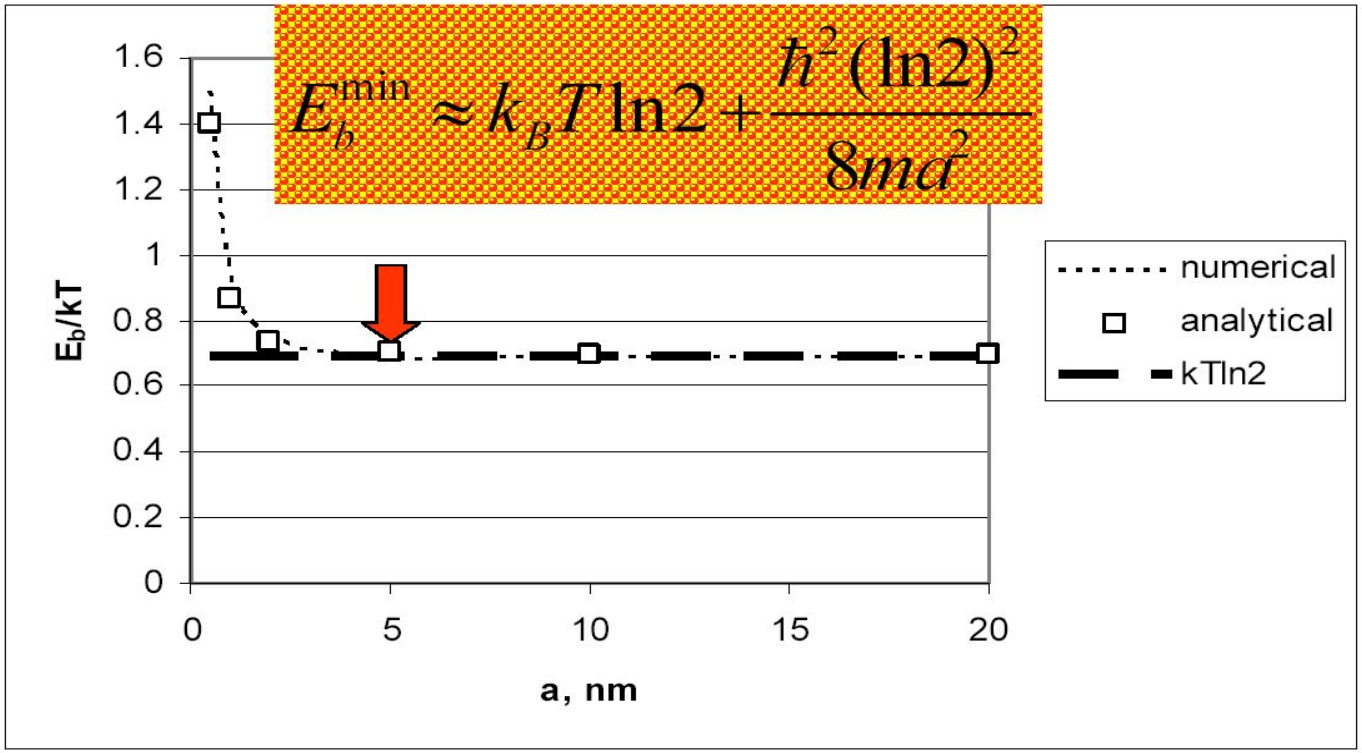






Zhibin Ren and Ramesh Venugopal (Purdue)
Dejan Jovanovic (Motorola, Los Alamos)

5 nm MOS is Theoretically Feasible



Minimum energy per switch operation as a function of minimum switch size

Paolo Gargini, Chairman of ITRS 2004

Более реалистические оценки мощности

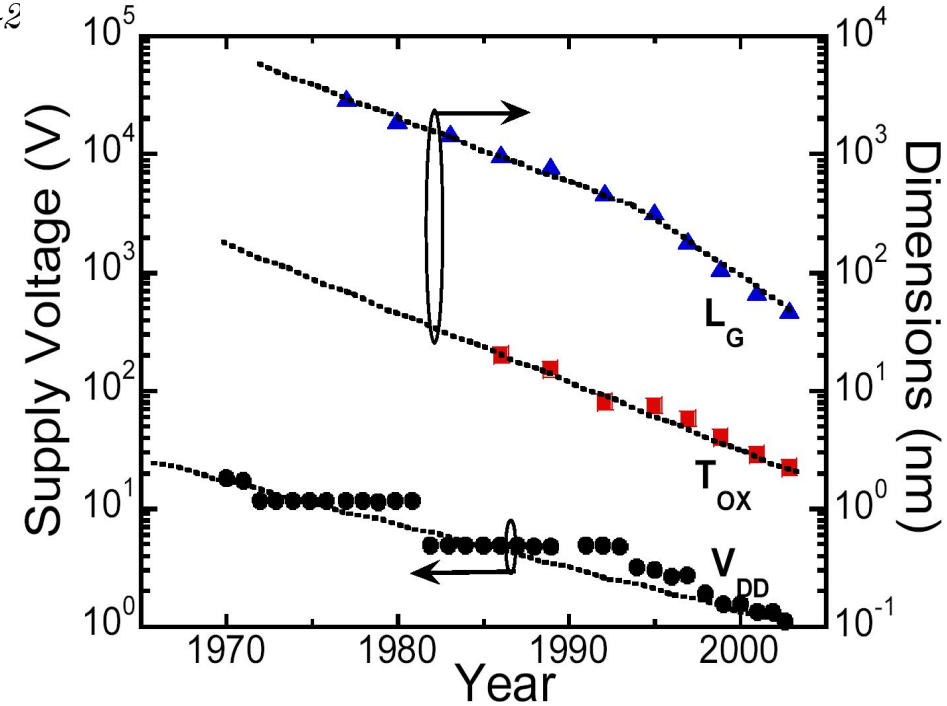
Сверху:

$$P = P_{\text{stat}} + P_{\text{dyn}} \approx 100\ Вт \cdot см^{-2}$$

где

$$P_{\text{stat}} = V_{DD} \cdot I_{\text{off}}$$

$$P_{\text{dyn}} = C \cdot V_{DD}^{2} \cdot f$$



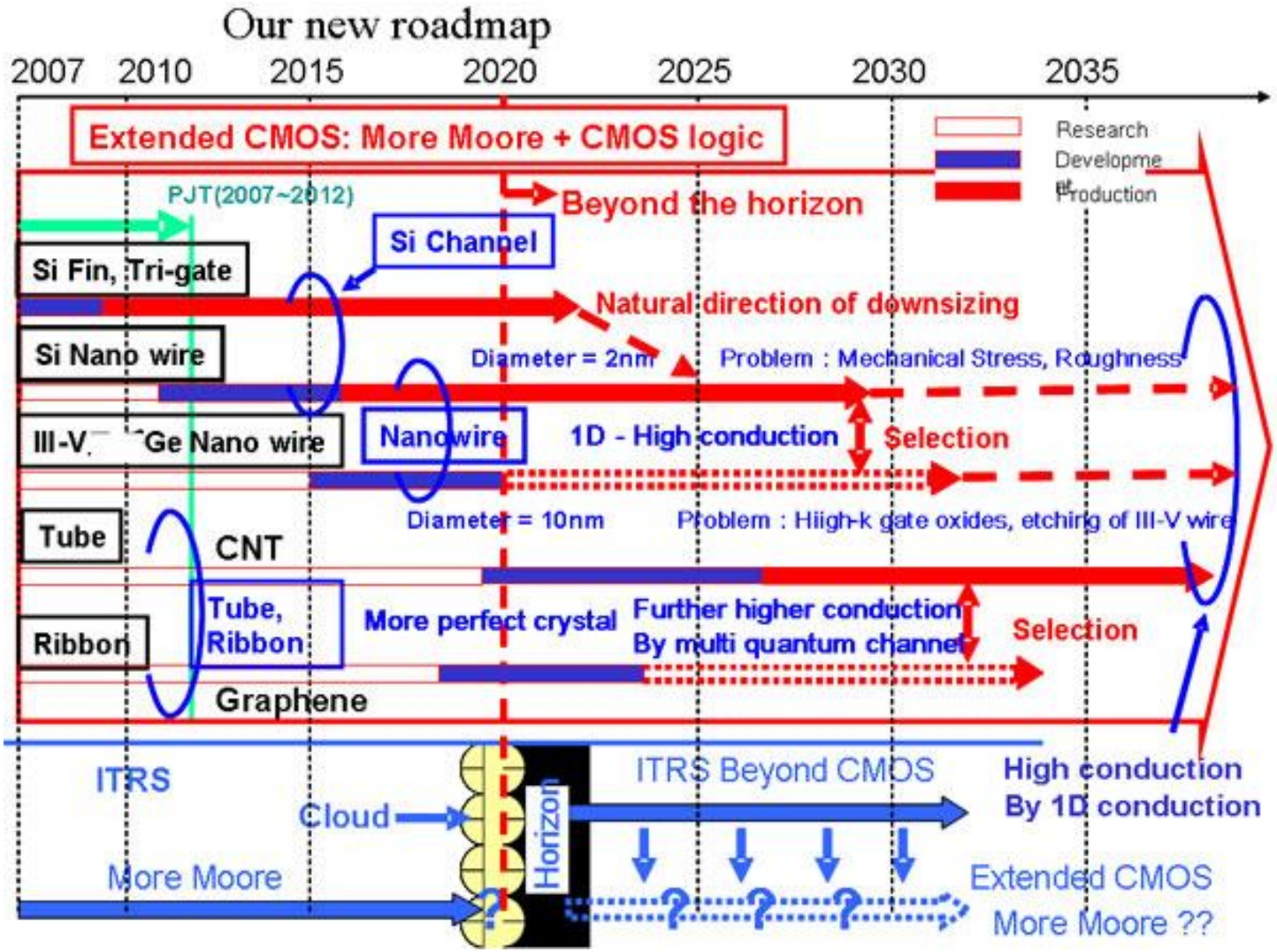
Снизу:

$$kTLn\left(\frac{N\tau_{mbf}}{\tau}\right) = C_L \cdot V_{\min}^{2}$$

$$V_{min} = \left(\frac{kTLn\left(\frac{N\tau_{mbf}}{\tau}\right)}{C_L}\right)^{1/2} \approx 10\ мВ \quad T = 300\ K,\ C_L = 0.4\ fF\ (t_{ox} = 1\ нм)$$

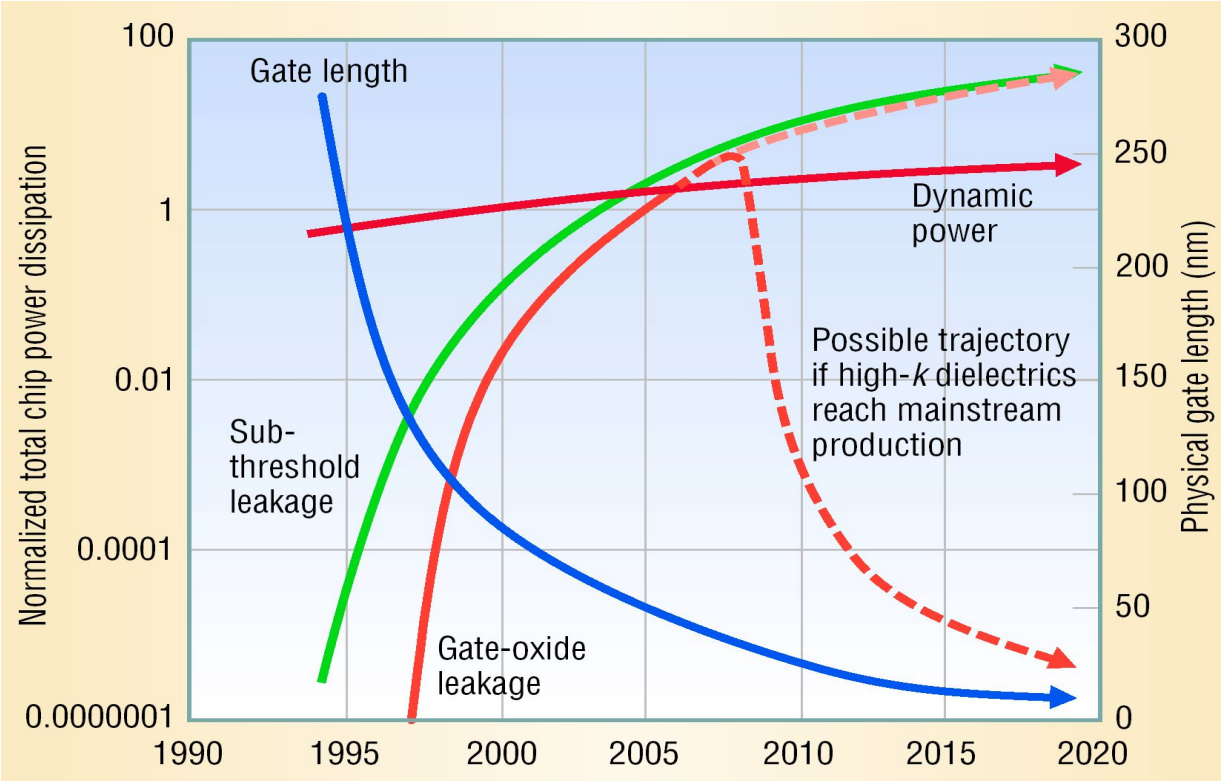
$$N = 10^9,\ \tau = 10\ ps,\ \tau_{mbf} = 1000\ h$$

The International Technology Roadmap for Semiconductors, edn. 2005



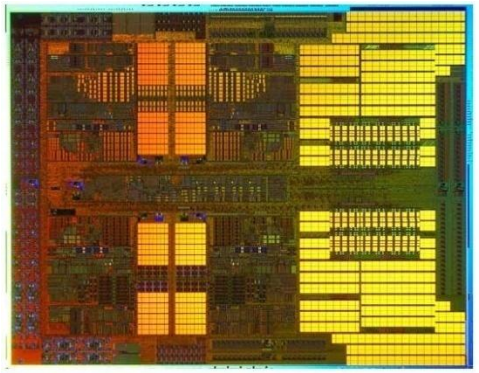
Hiroshi Iwai "Gate Stack Technology for the Next 25 Years"
4th International Symposium on Advanced Gate Stack Technology 25-28 September 2007 Dallas, Texas

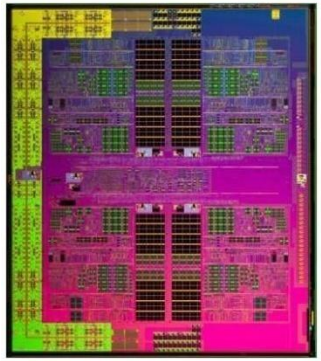
Изменение потребляемой мощности СБИС при переходе к high-k диэлектрикам

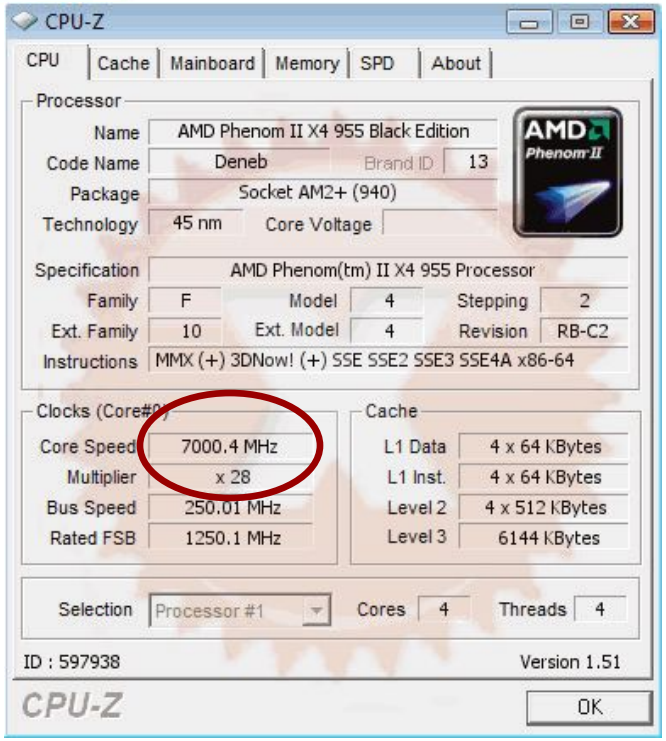


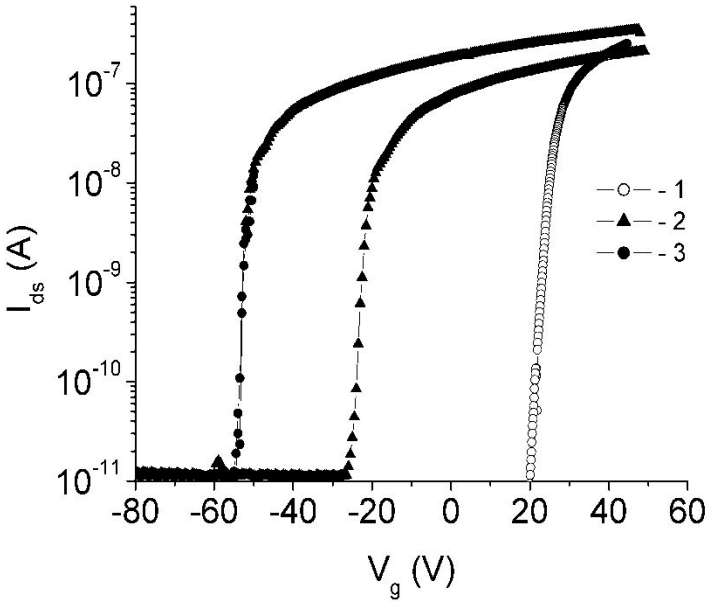
N.S.Kim, T. Austin, Leakage Current: Moore's Law Meets Static Power. IEEE Computer, pp. 68-75, 2003

Криогенная стабильность МП AMD Phenom II X4 и сдвиг сток-затворных характеристик КНИ нанопроволочных транзисторов









I_{DS}-V_{DS} кривые КНПТ (V_{ds}=0.15 V) измеренные при температуре :

1 – 300 K ;
2 – 14 K;
3 – 7.3 K.

Адсорбционный газоанализатор !

КМОП криогенная наноэлектроника?